International Journal of Enhanced Research in Science, Technology & Engineering
ISSN: 2319-7463, Vol. 5 Issue 4, April-2016

Low Power Class E Power Amplifier for Wireless Medical Sensor Network

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ABSTRACT

The objective of this research was to design a 2.4 GHz class E Power Amplifier (PA), with 0.18um Semiconductor Manufacturing International Corporation (SMIC) CMOS technology by using Cadence software, for health care applications. The ultimate goal for such application is to minimize the trade-offs between performance and cost, and between performance and low power consumption design. This power amplifier can transmit 23 dBm output power. The power added efficiency is 8.2% at 1dB compression point, the total power consumption is 0.15W. The performance of the power amplifier meets the specification requirements of the desired.

Keywords: Parallel, class E, power amplifier

1. INTRODUCTION

Wireless Sensor Networks (WSN) can be widely applied to solve a vast array of problems, under varied conditions [1]. By spatially distributing many devices to monitor the surrounding environment, WSNs can provide continuous, near-real time data over a large sampling area or population. WSNs can provide considerable efficiencies to otherwise costly tasks. For example, outpatient monitoring carries considerable cost, especially if applied to a large segment of the patient population. Cost-effective solutions can be established leveraging WSNs and the existing cellular communication infrastructure. Academic and hospital research is currently ongoing investigating such frameworks.

Due to current hardware limitations, healthcare application of WSNs are still in the early stages. Such devices require Food and Drug Administration (FDA) approval, which can be challenging and costly due to the requirement that the devices pass a number of safety tests. This has been historically challenging, with only a limited number of companies successfully building and fielding a device under full FDA approval [2].

WSNs consist of a number of networked elements, which are individually called sensor nodes. Sensor nodes contain a number of common hardware elements such as microprocessors, memory, batteries, MEMS sensors, antennas, etc. A major design constraint for medical applications is that - since it is a consumer application - designs must meet functional requirements while being cost-effective [2]. In order to implement networks with a large number of nodes (for example with one node per patient), each node must be low cost. For many applications, WSN nodes have challenging power requirements, as well. Typically, each node must offer long working cycles without battery recharging. This drives most sensor node designs to be ultra-low power devices. Achieving this low power performance at low cost are critical to making such sensor networks feasible[3].

In this pursuit, designs can reduce costs by leveraging the rapid development and widespread use of wireless systems. The wireless hardware industry, driven by global consumer demand, already strives for low cost, compact designs with flexible functionality. Transceivers systems are typically implemented in the Complementary Metal-Oxide Semiconductor (CMOS) technology. CMOS is a highly matured and well-understood technology. Advanced CMOS technologies can integrate the digital, analog and Radio Frequency (RF) components on a single, tiny chip.

2. BACKGROUND INTRODUCTION

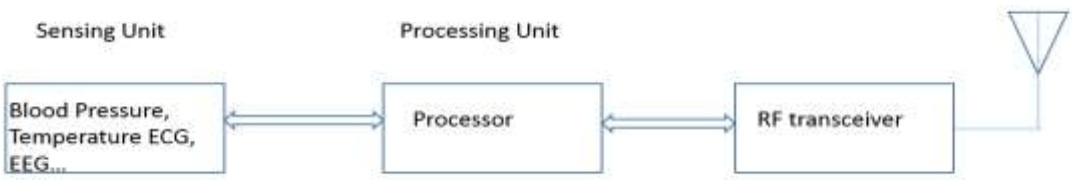


Figure 1. Block diagram of a typical sensor node.

In a wireless sensor network, as seen in the figure 1 below, each device is capable of monitoring, sensing, and/or displaying information. A sensor node is capable of gathering sensory information, processing it in some manner, and communicating with other nodes in the network.

Fig.1 shows that the basic sensing node can collect the physiological signals (e.g.: such as EEG, ECG, body temperature, blood pressure, heart beat etc.), when attached to a human body [2]. The processing unit processes all the sensed signals, then sends out the data based on communication protocols. All the processed data will be transmitted through a wireless link to a portable, personal base-station. Doctors can then obtain all the patients' data through the network [3] [4] [5].

The main challenge for such sensor node is the high power consumption of portable devices. A solution to this challenge is the integration of the portable devices' digital and RF circuitry into one chip [6] [7].

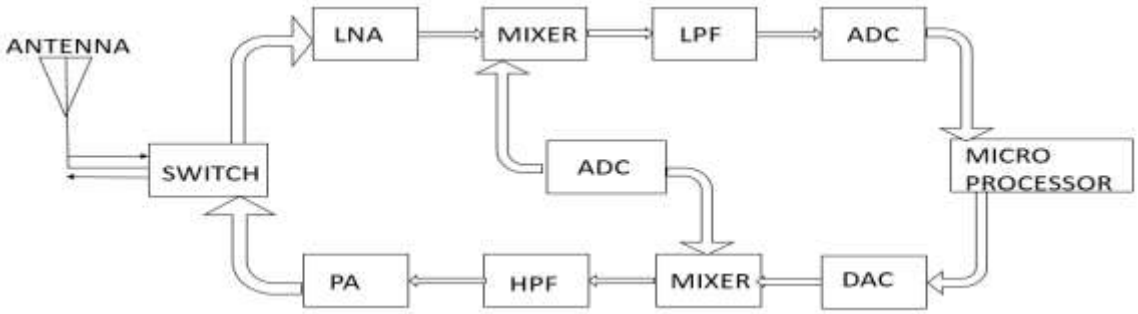


Figure 2. Block diagram of a transmitter

As seen in the figure 2, a sensor node has many blocks. In the transceiver chip, a power amplifier is the last RF block in the transmit chain [6]. The power amplifier consumes the most DC power in the transceiver, and hence the power amplifier's efficiency largely determines the overall transmitter-receiver system performance. For a low-power design, it is necessary to design a high efficiency power amplifier for the whole system.

On the other hand, the radio frequency section of a wireless terminal is always a major contributor of the whole chip power consumption, and building monolithic Radio Frequency (RF) transceivers in the CMOS process is always challenge, because of the process' physical limitations [8]. Therefore, to design and implement monolithic, high efficiency transceivers in low-cost CMOS, the key is to improve the whole wireless system's performance; more precisely, by optimizing the power consumed by RF circuitry. In order to meet the standards, the PA is designed as shown in Table 1. Switch mode class-E power amplifiers offer the optimal solution in terms of efficiency and can easily obtain sufficient linearity. A power switch mode modified driver can be implemented for parallel class-E power amplifiers to improve the RF performance. In this paper a parallel class-E power amplifier with a modified driver stage is implemented for the IEEE 802.11b standard.

TABLE 1: PA design requirement.

Parameter	Target
Output Power	18dBm
PAE	30%
Stability	>1
S11	-10 dB

3. PA Design

Over the past 30 years, research on CMOS radio-frequency (RF) front-end circuits has progressed extremely quickly. The ultimate goal for the wireless industry is to minimize the trade-offs between performance and cost, and between performance and low power consumption design [8].

The proposed Class E amplifier has low output power and good linearity based on the IEEE 802.11b communication protocol. The class E power amplifier topology is shown in figure 3.

A. PA Deisgn

The single ended class E power amplifier configuration is as shown in figure xxx. This configuration consists of a power supply Vdd, an RF choke inductor L2, a switch Q1 parallel with a capacitor C3, a resonant circuit L3, C3 and a load RL. The switch Q1 can be periodically turned on and off. In the other words, Q1 is on for a half cycle and off in the other half. L3 and C3 forms a resonant circuit. The resonant frequency of the output loop has different values when Q1 is on and off. Ql is designed with a large gate width [9]. This generates harmonic distortion. The capacitor C2 tried to keep the voltage across the switch relatively low after the drain current is reduced to zero [9].

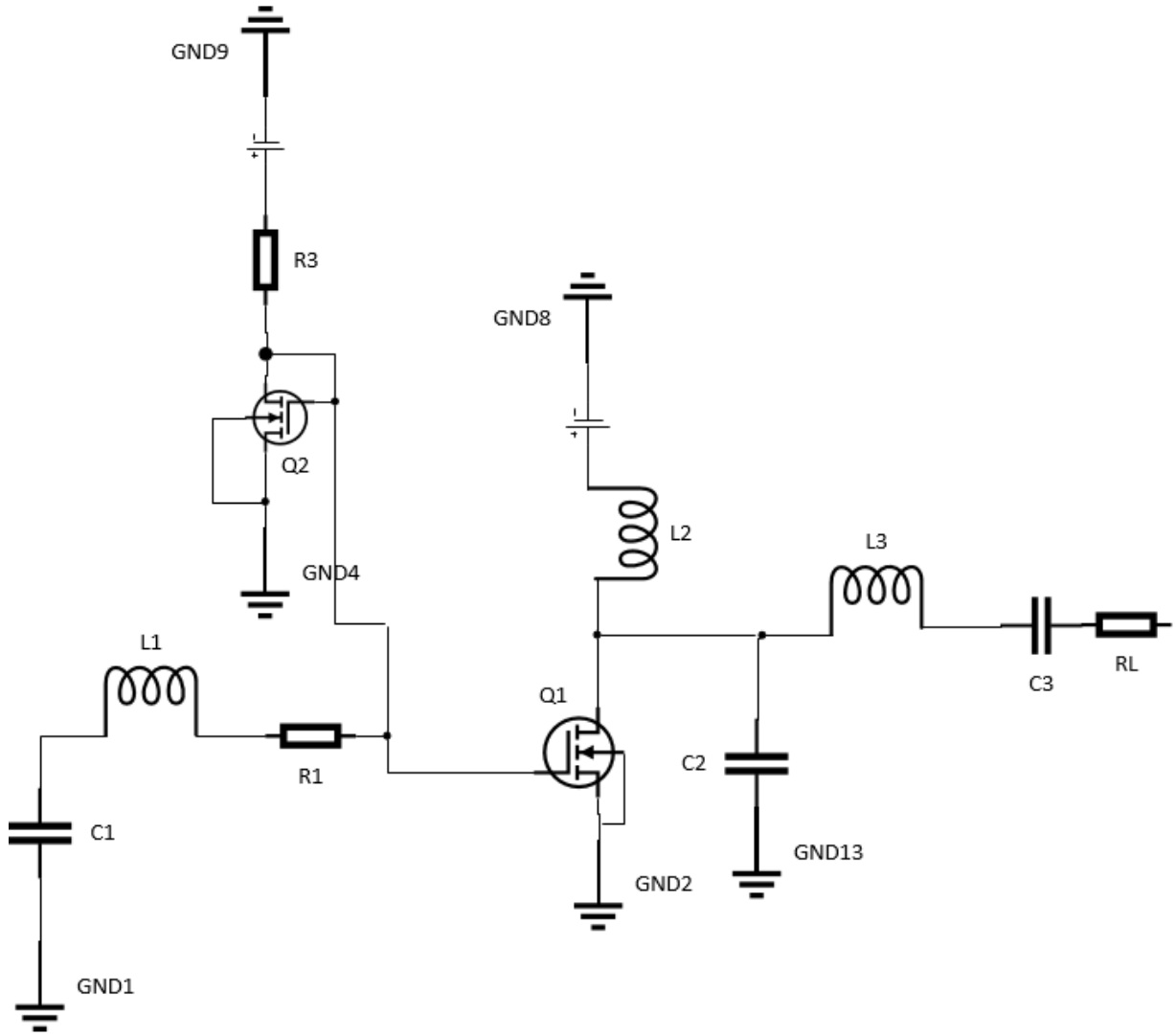
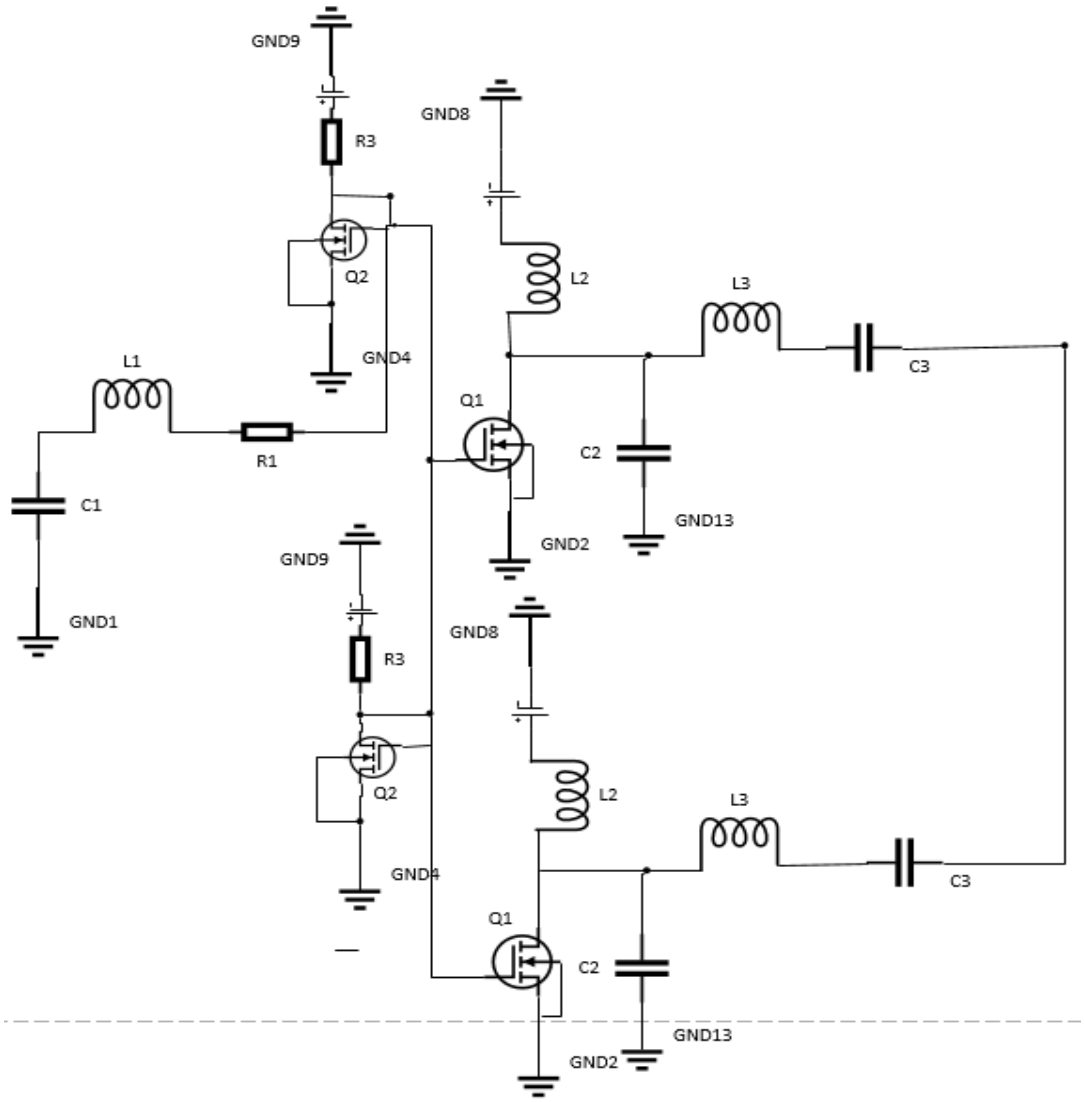


Figure 3. Block diagram of a single eneded class E power amplifier

Parallel power amplifier topologies, for the same output power, consume less RF input power than a single ended PA design. The tradeoff, however, is that parallel designs require more components and as a result cost more to manufacture. A detailed schematic of a parallel power amplifier is shown in Figure 4. The detailed schematic shows that the parallel PA consists of two single ended power amplifiers in parallel. Parallel PA operation is same as single ended power amplifier operation [7]. The capacitor C1 should be large enough to minimize the power loss at the gate terminal. Inductor L1, parallel with capacitance seen at the transistor Q1 input is tuned at the fundamental frequency of desired RF signal. Resulting design values can be shown in Table 2 for both single ended and parallel class E PA.



(a)

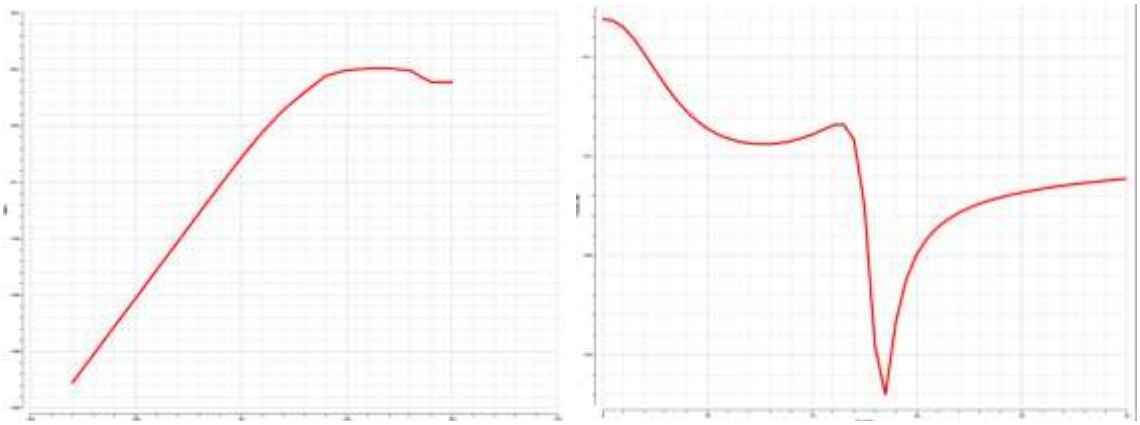
Figure 4. (a) Schematic of parallel class E power ampfliier.

TABLE 2: PA single stage component.

Parameter	Size (Unit)
Q1	W/L=03um/0.6um (f=66,m=24)
Q2	W/L=0.8um/0.6um (f=4,m=2)
R1	10.5 Ohm
R3	3.8 KOhm
L1	36 nH(Q=20)
L2	20 nH (Q=20)
L3	2 nH (Q=20)
C1	240fF
C2	1.1 pF
C3	600 fF

B. Single –ended Class E PA Design Simulation

As seen in figure 5 (a), the output power is 20 dBm. As seen in figure 6(b), the frequency is at 2.4 GHz the S11 is less than -10 dB, also, the total power of the PA is 3.4 W.



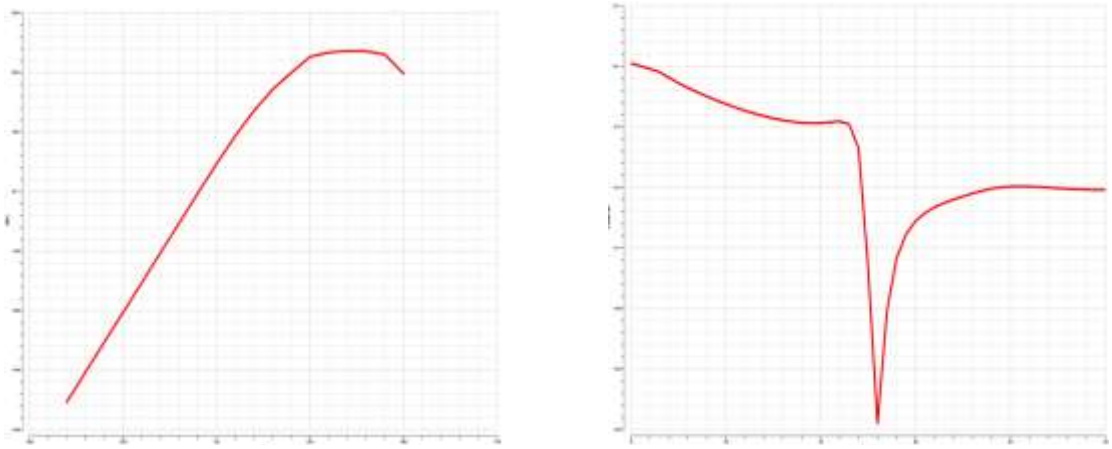
(a) (b)

Figure 5. (a) PA output (b) S11

C. Parallel PA Design Simulation

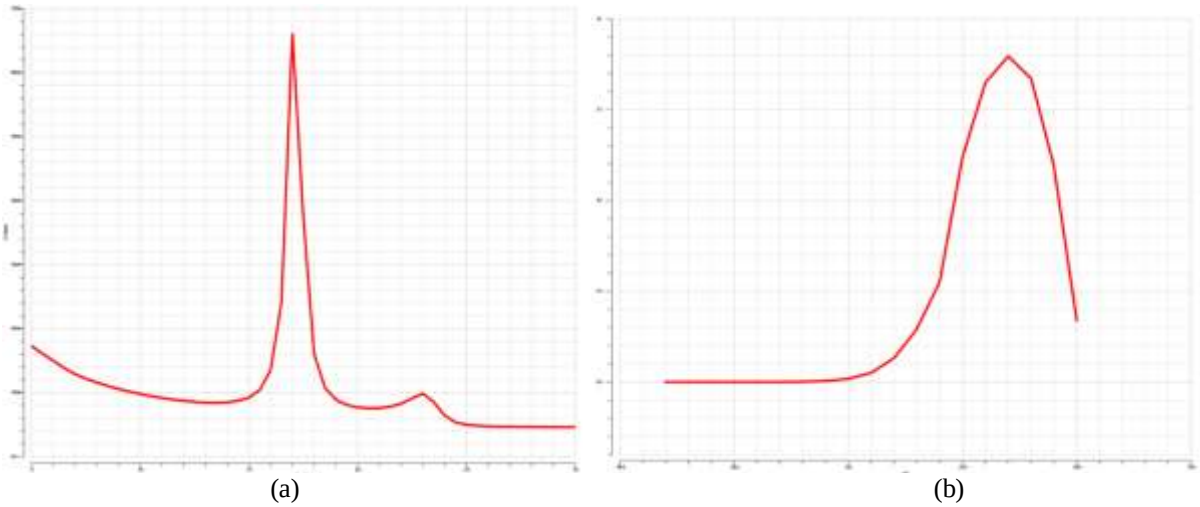
As seen in figure 6 (a), the output power is 23 dBm. As seen in figure 6(b), the frequency is at 2.4 GHz the S11 is less than -10 dB, also, the total power of the PA is 3.4W.

As seen in figure7 (a), Kf is larger than 1 for all frequencies from 1 to 3 GHz, so this circuit is totally stable. And the PAE is 8.2% at input power 0 dB.



(a) (b)

Figure 6. (a) PA output (b) S11



(a) (b)

Figure 7. (a) Kf (b) PAE

4. CONCLUSION

This paper describes the method of designing and simulating power amplifier using cadence software based on SIMC CMOS process 180nm technology. This PA is used for sensor networks. This research is still in the early stages of development of a low cost and low power device. In order to reach the performance that is needed, the PA process uses group III and IV elements. This circuit meets the scheduled requirements for the CMOS process, but it still has room to improve performance metrics. When the sensor is coupled with communications technologies such as mobile phones and the Internet, the sensor network constant information flow between individuals and their doctors. Such low cost and low power device can save a lot of hospitalization resources. To realize this, future improvement is needed.

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