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Use of Application Specific Integrated Circuits in Electronics Engineering

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Abstract: In this paper, the author has enlighten the use of Application Specific Integrated Circuits in the field of Electronics Engineering. Application Specific Integrated Circuits or ASICs are non-standard integrated circuits that are designed for a specific use or application. Here a complete system or product is integrated onto a chip and virtually no other components are required. The cost of designing an ASIC is very high and therefore they tend to be reserved for high volume products. But ASICs can be very cost effective for many applications where they are produced in large scale.

Keywords: ASCIs, applications, circuits, electronics engineering.

Introduction

An application-specific integrated circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed to run in a digital voice recorder or a high-efficiency Bitcoin miner is an ASIC. Application-specific standard products (ASSPs) are intermediate between ASICs and industry standard integrated circuits like the 7400 or the 4000 series.

As feature sizes have shrunk and design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 gates to over 100 million. Modern ASICs often include entire microprocessors, memory blocks including ROM, RAM, EEPROM, flash memory and other large building blocks. Such an ASIC is often termed a SoC (system-on-chip). Designers of digital ASICs often use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

Field-programmable gate arrays (FPGA) are the modern-day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs or lower production volumes, FPGAs may be more cost effective than an ASIC design even in production. The non-recurring engineering (NRE) cost of an ASIC can run into the millions of dollars.

Since the 1980s, product offerings of the typical semiconductor manufacturer have undergone dramatic changes. Memories, Microprocessors, and other traditional high volume standard products that are still available are now referred to as "commodity products". In addition, current standard product portfolios include a significant proportion of so-called Application Specific Standard Products (ASSPs). These ASSPs differ from commodity products through the incorporation of value-added features for specific market segments (e.g. complete SCSI controllers targeted for workstations). Furthermore, ASSPs from different vendors may have similar functionality but they are seldom pin-for-pin compatible; resulting in intensive "design-in competition" among vendors offering comparable solutions to the same problem. Figure 1 illustrates this hierarchy in the present Integrated Circuit market. The introduction of the ASSP designation is a natural result of semiconductor manufacturers use of the ASIC design methodology for standard products. However, this points to a problem of accuracy with the current use of the term ASIC. ASIC chips are not generally just application specific, they are customer specific. It can be argued that customer programmable logic devices are the only true ASICs. To compound this problem, the term is used differently by different people in different contexts. ASIC is defined variously as gate array, any custom, semi-custom, or programmable technology, and as a design methodology.

Needs & Approach for ASCIs

ASICs are a fundamental component needed for instrumentation for all three High Energy Physics frontiers. Integrated circuits allow high channel density, improve analog performance (e.g. noise, speed), enable data reduction, lower power dissipation, reduce cabling, reduce mass, lower cost and in many applications even make the experiment possible. Needs depend on the application but are in the area of high-speed waveform sampling, fast timing, low-noise high-dynamic-range amplification and shaping, high-speed digitization, digital data processing, high-rate data transmission, low temperature operation, radiation tolerance, and low radioactivity. Just as one example in the energy frontier, luminosity upgrades in the HL-LHC era present significant ASIC challenges to the in-detector electronics and will require a number of new ASICs which will need R&D in several above performance areas.

A wide range of fabrication processes are available and ASICs are designed in the most suitable and cost effective process to achieve the desired performance. For ultra low-noise high-dynamic range applications where analog performance is key or signal channel density is not the driving factor, 130nm to 250nm CMOS technologies are currently preferred. The fabrication cost is also much lower compared to smaller feature technologies. For application where large number of small pixels are desired and where digital processing within each pixel is an option (like for some of the LHC detector subsystems), 65nm technology is currently preferred although more challenging in the design and having a much large fabrication cost. Smaller feature processes also result in higher speed circuits. Cost of CAD tools is a factor especially in international ASIC design collaborations where tools are specified or for circuits where comprehensive verification tools are needed. Cross-cutting design challenges for ASICs are novel, better performance circuitry.

Other areas of research are circuits operating at non-commercial temperatures, in a highradiation environment, or in non-standard processing (e.g. MAPS, power conditioning, high-voltage). Some R&D in non-bulk CMOS processes as for example SOI or SiGe is taking place. Density can be improved by going to 3D assemblies; this technology requires more research and development especially to be able to achieve the yield and reliability required.

In general the ASIC design groups usually benefit from designing ASICs for non-HEP applications (e.g. photon science, nuclear science, medical applications, WFO).

Literature Review

The initial ASICs used gate array technology. Ferranti produced perhaps the first gate-array, the ULA (Uncommitted Logic Array), around 1980. An early successful commercial application was the ULA circuitry found in the 8-bit ZX81 and ZX Spectrum low-end personal computers, introduced in 1981 and 1982. These were used by Sinclair Research (UK) essentially as a low-cost I/O solution aimed at handling the computer's graphics. Some versions of ZX81/Timex Sinclair 1000 used just four chips (ULA, 2Kx8 RAM, 8Kx8 ROM, Z80A CPU) to implement an entire mass-market personal computer with built-in BASIC interpreter.

Customization occurred by varying the metal interconnect mask. ULAs had complexities of up to a few thousand gates. Later versions became more generalized, with different base dies customised by both metal and polysilicon layers. Some base dies include RAM elements.

During the 1980's, Full Custom and Application Specific Integrated Circuit designs were approached from two quite different directions. ASIC design focused on meeting time-tomarket and customer specific requirements. ASIC design methodologies used chips containing arrays of prefabricated gates (gate arrays), or chips based on libraries of standard function cells (standard cell designs). These designs sacrificed density but allowed the customer to perform major portions of the design in-house; albeit with significant help from the semiconductor manufacturer. Full-custom or hand-crafted IC design addressed maximum density and performance for high-volume standard products. These full custom chip designs were the sole purview of the semiconductor manufacturers who targeted only the largest markets; frequently providing customers with multiple sources for most products.

An even more gray area is created by the previously discussed ASSPs. Although they are built using traditional ASIC technology, they are sold like standard parts. Nonetheless, the term ASIC is still quite useful. In addition to describing gate array, standard cell, and PLD chip designs, ASIC describes a methodology (or group of methodologies) for designing electronic systems, and it describes a technology (or group of technologies) used to build electronic systems. Most of today's flexible and cost effective electronic systems are designed using ASIC methodologies and built using ASIC technology. It is clear that a wide range of Integrated Circuit (IC) design options are available for electronic system

construction. Many factors must be considered in order to make informed choices about the chips that we purchase, specify, or design. The remainder of this introduction provides a broad comparison of the ASIC and programmable logic technologies, and identifies both technical and economic selection criteria. Section II provides an overview of the semiconductor processing technologies in use today, and provides a brief comparison of technology attributes. In Section III an in-depth evaluation of field-programmable logic devices is presented together with examples of currently available commercial chips. Sections IV and V present information about the more traditional gate array and standard cell ASIC design methodologies. Finally, Sections VI and VII discuss system implementation and application issues including ASIC packaging, behavioral modeling, design for testability, and mixed-signal design.

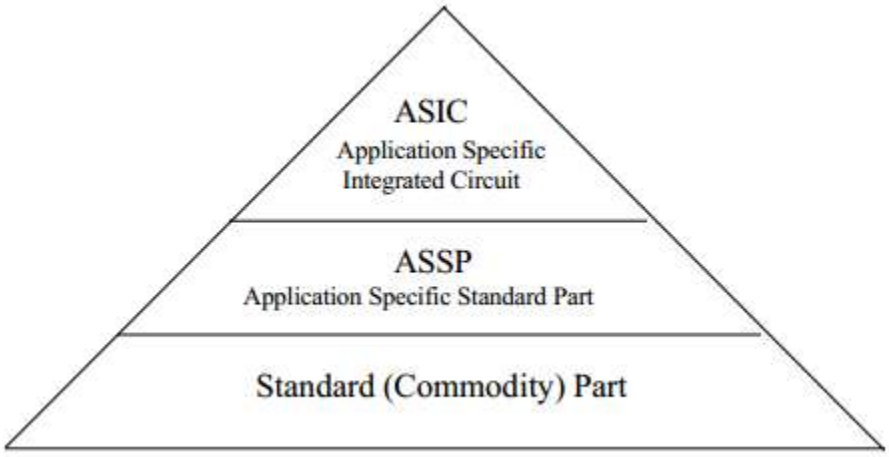

Figure 1: VLSI Market Hierarchy

Design Flow Analysis for an ASIC

A design flow is a sequence of steps to design an ASIC. Following are the steps of ASIC design:

1. Design entry: Using a hardware description language (HDL) or schematic entry, design is entered into an ASIC design system.

2. Logic synthesis: Using HDL (VHDL or Verilog) and a logic synthesis tool a netlist is produced. Netlist is a description of the logic cells and their connections.

3. System partitioning: In this step, a large system is divided into ASIC-sized pieces.

4. Pre-layout simulation: Functioning of the design is checked if it is working correctly.

5. Floor planning: The blocks of the netlist are arranged on the chip such a way that they take optimum space. In floor planning, distribution of connections and inter-effects of electrical parameters are also considered.

6. Placement: The locations of the cells in a block are decided.

7. Routing: The connections between cells and blocks are made.

8. Extraction: The resistance and capacitance of the inter-connects are determined.

9. Post-layout simulation: After the interconnections have been made, working of the design is tested.

Type of ASIC Designs

This section introduces the range of options and styles available for integrated circuit design. Although the bulk of this chapter will focus on the programmable logic design style, this section places programmable logic in context alongside the alternate design techniques. The following sections are loosely organized in order of decreasing design investment (non-recurring engineering costs) and corresponding maximum chip complexity.

Full Custom Design

In the classic full custom design style, each primitive logic function or transistor is manually designed and optimized. This results in the most compact chip design with the highest possible speed and lowest power dissipation. However, the initial investment or Non-Recurring Engineering (NRE) cost is highest compared to all other design styles. The designer must manipulate the individual geometric shapes which represent the features of each transistor on the chip; hence the often applied term for full custom design: "polygon pushing". A relatively simple 3000 gate design might require the handling of 300,000 rectangles per chip. Although this design style was used exclusively in early ICs, engineers rarely use it for today's ASICs due to the high engineering costs and low designer productivity. Productivity for full custom logic designs is typically only 6 to 17 transistors per day. The exception is in high volume commodity products such as memories which must be hand-crafted to meet density and performance requirements. In addition, at least portions of high-end products such as microprocessors are full custom designed for performance reasons. Worldwide sales of full custom ASIC designs are predicted to grow only slightly from the current level of $2.7 Billion to $2.9 Billion in 1998 (a declining market share from 23% to 16%).

Standard-Cell–Based

ASICs ASIC manufacturer creates functional blocks with known electrical characteristics, such as propagation delay, capacitance and inductance. Utilizing these functional blocks, standard cell of very high gate density and good electrical performance is designed. This gives a high degree of flexibility, provided that standard functions are able to meet the requirements. The significant advantage in Standard-Cell–Based ASICs is that this uses the manufacturer's cell libraries that have been used in potentially hundreds of other design implementations. Thus, there is very low risk associated than full custom design. Standard cells produce a design density that is cost effective, manufacturing time is also less (about eight weeks) and they can also integrate IP cores and SRAM effectively.

Gate Array Design

Full custom and standard cell design methodologies require custom chip fabrication using a complete set of unique masks which define the semiconductor processing of the design. Thus, both the NRE cost for the mask set and the design turn-around time through the foundry are quite high. As an alternative, a chip design can be created using a custom interconnection pattern on an array of uncommitted logic gates (i.e. a gate array). Wafers of chips containing the uncommitted logic gate arrays can be pre-fabricated up to the point of the final metalization steps which create the logic personalization. Compared to standard cell or full custom designs, the design turnaround time and cost are reduced because only the top level interconnect and contact mask steps (2-5 masks) need to be applied. Several other advantages of these "mask programmed" gate arrays relate to the economies of scale for this design style. Wafer costs are low because many different customer designs can be created from the same base wafer design. Similarly, foundry packaging and test costs are low due to standard pin-outs and common test fixtures which can be used for multiple designs. Section IV will describe gate array design in more detail.

Field Programmable Logic

A field programmable logic device is a chip whose final logic structure is directly configured by the end user. By eliminating the need to cycle through an integrated circuit production facility, both time to market and financial risk can be substantially reduced. The two major classes of field programmable logic, Programmable Logic Devices (PLDs) and Field Programmable Gate Arrays (FPGAs), have emerged as cost effective ASIC solutions because they provide low-cost prototypes with nearly instant "manufacturing". This class of device consists of an array of uncommitted logic elements whose interconnect structure and/or logic structure can be personalized on-site according to the user's specification.

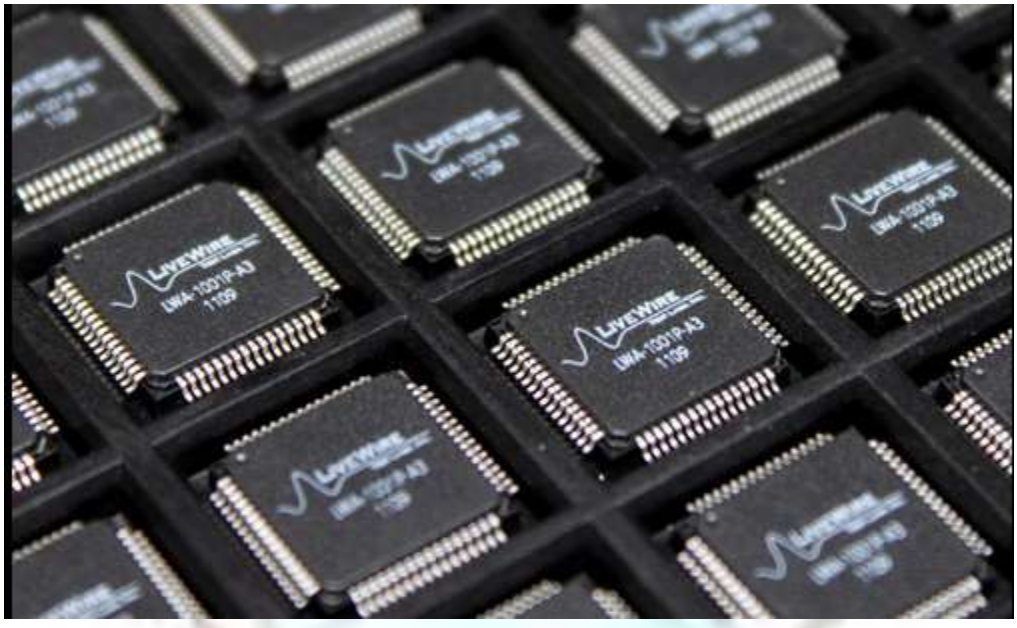

Figure 2: A tray of Application-specific integrated circuit (ASIC) chips

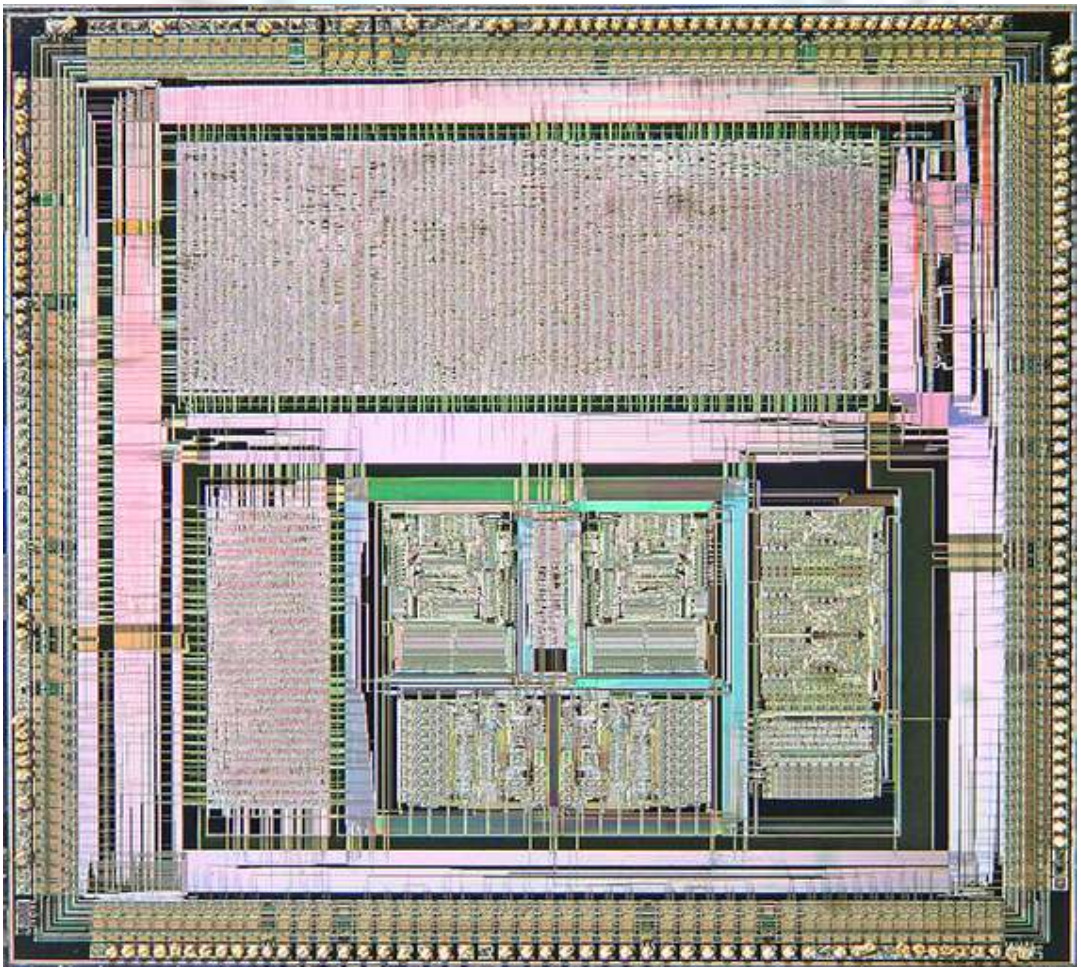

Figure 3: Custom ASIC (486 chipset) showing gate-based design on top and custom circuitry on bottom

Advantages of an ASIC

Following are advantages of an ASIC:

1. Small in size: An ASIC is designed with proper floor planning. So, the size of an ASIC designed for a specific application is always smaller as compared to other programmable devices. Small size consequently leads to advantages in speed and power consumption.

2. No routing Issues: There are no any issue of routing for the end user in ASIC, once it is designed.

3. No timing Issues: Digital logic switching, analog effects and communication between blocks in the chip is faster in ASIC. Any configurable hardware must meet the timing requirement for the efficient operation of the circuit. Longer wires between components may affect the timing. Sometimes, over timing or under timing the new added design may yield erroneous result. An ASIC doesn't have this problem.

4. Less Power Consumption: ASIC consumes less power because logic operations are done within a chip; since smaller components have much smaller parasitic resistance, capacitance and inductance.

5. Consistence and Reliable: An ASIC is consistent and reliable in its performance since it is designed by skilled designers to work for a specific task. Also, the probability for failure and impact of external environment are much less in integrated circuits. The lifetime of ASICs is much longer as they are IC based.

Conclusion

An ASIC is a unique type of integrated circuit meant for a specific application. An ASIC can no longer be altered once created FPGA is alterable. An ASIC wastes very little material, recurring costs are low. A certain number of components are always wasted. Cost of ASIC is low only when it is produced in large quantity. ASICs can't be used to test FPGAs. ASICs are tested on FPGA before implementing. ASICs are not suitable for research and development purposes, as they are not reconfigurable.

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