Wireless Sensor Network Applications in Low Power Circuits

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Abstract: As the CMOS technology continues to scale down into the nano-scale regime, robustness of the circuit with respect to process variation and soft error are becoming major obstacles for circuit designers. Storage elements (SRAM, flip-flops) are particularly vulnerable to process variation and soft errors. Thus, in this work, we have focused on storage elements to improve the yield loss in SRAM due to process variations and to design a soft error tolerant flip-flop. SRAMs are particularly vulnerable to failures due to process variation resulting in reduced yield. The main problem with SRAM is the conflicting requirements for read stability and writes ability. In this work, we propose designs to overcome conflicting trade-off between read and write stability. Furthermore, new SRAM cells, namely 11TSRAM, PMOS access transistor SRAM, are proposed with capability of working at near threshold voltages, properly. The effect of body-biasing on SRAM cell is explored to show improvements from body-biasing in sub-threshold regions. Results show at least 30% improvement in read noise margin for proposed SRAM cells while write margin is improved. Furthermore, to overcome short channel effect, different candidate transistor structures have been investigated to replace the bulk MOSFETs. Among them, FINFET is considered to be a promising candidate for scaled CMOS devices in sub-22-nm technology nodes. In this work, by introducing a new device, the read and write stability for SRAM is improved by 20% and 9% respectively, while performance is improved by 56%compared to conventional designs. we study the double-gate FINFET SRAM technology-circuit design space to understand the interplay of device short-channel-effect (SCE), SRAM area, access time, soft error immunity, stability under process variations and leakage. Several Flip-Flop designs are designed to reduce power in DSP applications. Simulation results show 40% improvement in total power saving for some DSP applications such as FIR filters and other DSP applications. Design challenges in submicron CMOS technology are investigated in details for sub-threshold designs for wireless sensor network applications. In this work different CMOS model such as ST Microelectronic, TSMC and IBM models are used for different application.

INTRODUCTION

CMOS devices have been scaled down aggressively in the last few decades resulting in higher integration density and improved performance. However, due to short channel effects, threshold voltage (Vth) scaling, oxide thickness scaling and increased doping density, the "off" current in the devices has increased drastically with technology scaling. Hence, as we are approaching the end of the silicon roadmap, controlling leakage current is becoming a major problem. Moreover, statistical variations in process parameters, such as device structure (channel length, oxide thickness, width etc), location and number of dopants in channel (random dopant fluctuation), is increasing with technology scaling. The variation in process parameters results in large distribution in delay and leakage and significantly reduces robustness of a circuit. Hence, large leakage current and increasing process variations have emerged as two major obstacles for designing CMOS circuits (logic and memory) at the end of silicon roadmap. Smaller transistors are inherently faster and consume less dynamic power. However, when millions of transistors are integrated together to create a complex VLSI system, we observe several new challenges threatening the reliability of computation. Some of them are as follows:

Leakage Power: With ever-increasing operating frequency and more transistors on a single die, switching power has increased significantly (Fig.1.1). By scaling the devices to sub-50nm regimes, controlling over the channel and second order effects such as short channel effects, DIBL, narrow width effect etc., has become less. Furthermore, by technology scaling, leakage components increase significantly. Fig.1.2 shows the leakage power components and the percentage of leakage power for different technology nodes. Both dynamic and leakage power consumption affect the reliability of the underlying devices and reduce the battery lifetime of handheld devices. In another word, ION/IOFF ratio decreases with scaling technology. Especially, for ultra low voltage applications such as wireless sensor nodes, using techniques to reduce the leakage current is crucial due to a very low ION/IOFF ratio in near threshold or sub-threshold regions.
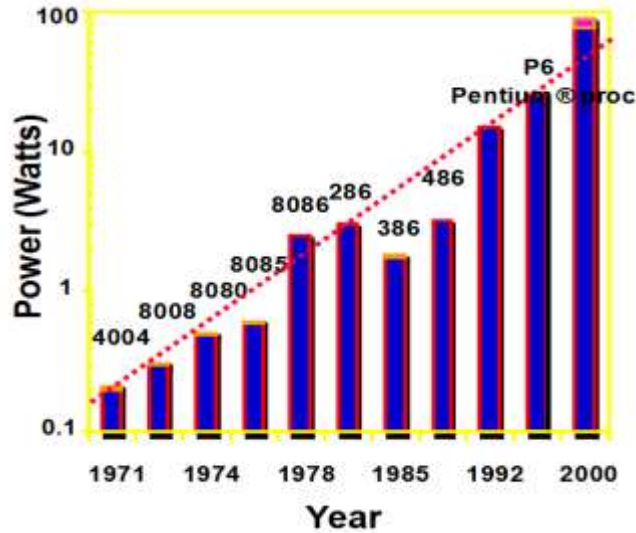
Fig. 1. Increasing power over technology generations [Intel]

Process Variation: Sub-wavelength lithography has led to large variation in transistor geometries (L;W; TOX) and the flat-band voltage (VFB). Process variation effects are more stringent in small size devices. Variations in channel length, channel width, oxide thickness, threshold voltage, line-edge roughness, and random dopant fluctuations are the sources of the inter-die and the intra-die variations in process parameters [the random variations in the number and location of dopant atoms in the channel region of the device resulting in the random variations in transistor threshold voltage (RDF)]. One of this inter die effects is threshold voltage variations due to the changes of a single transistor (e.g. threshold voltage increases if temperature is reduced). However, intra-die variations may be different from one transistor to another (i.e. increase in Vth for one device on the other hand decrease in threshold voltage for another). An example of the systematic intra-die variation can be the change in the channel length of different transistors of a die that are spatially correlated.
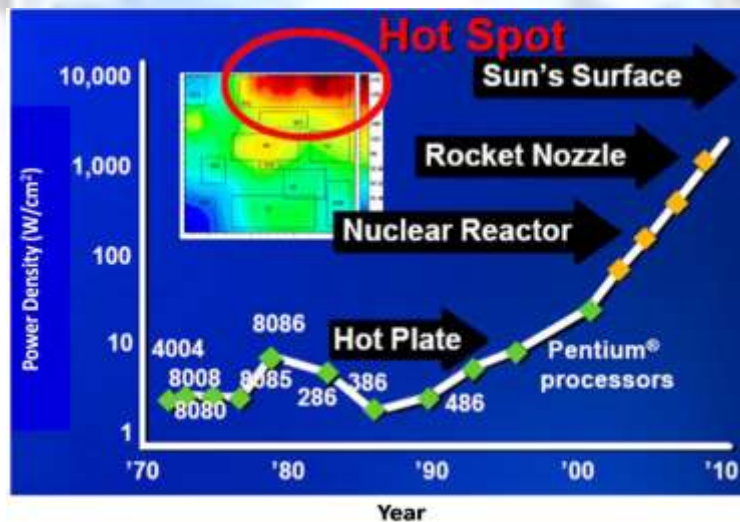

Fig. 2. Increasing power density with technology scaling [Intel]

Occur Due To: (a) an increase in the cell access time (access failure), (b) unstable read/write operations (read/write failure),or (c) failure in the data holding capability of the cell at a lower supply voltage. Body-biasing has been used for mitigating the impact of inter-die process variation and reducing the parametric failures [1]. However, it has been observed that the effectiveness of body-biasing reduces with technology scaling [2]. Different challenges in ultra low supply voltage, especially for storage circuits, are investigated in this dissertation. Unfortunately, for lower supply voltages the effect of

process variations increases significantly. Therefore looking at process variations in different designs, especially for very low voltages is interesting.

<h2 align="center">Leakage-Tolerant Logic Circuit Design</h2>

High fan-in compact dynamic gates are often used in high performance critical units of microprocessors. However, the use of wide dynamic gates is strongly affected by subthreshold leakage and noise sources [25]. This is mainly due to decreased threshold voltage that results in exponentially increased leakage currents in scaled technologies. To reduce power consumption, supply voltage scaling is used across technology scaling. However, threshold voltage needs to be scaled down as well to maintain transistor overdrive for large ON currents. Less threshold voltage means smaller gate switching trip point in domino circuits. Smaller trip points make the domino circuit more prone to inputnoise. Moreover, excessive leakage can discharge the precharge (dynamic) node of a domino circuit resulting in a logic failure (wrong evaluation). In addition to reduced trip pint and increased leakage, other noise sources such as supply noise and crosstalk noise also increase by technology scaling, further degrading the robustness of domino logic.

Conventional approach for improving the robustness of domino circuits is keeper transistor upsizing. However, as the keeper transistor is upsized, the contention between keeper transistor and NMOS evaluation network increases in the evaluation phase. Such current contention increases evaluation delay of the circuit and increases power dissipation. Thus, keeper upsizing trades off delay and power to improve noise and leakage immunity. Such trade-off is not acceptable because it may make the circuit too slow or too power hungry. There are techniques proposed in the literature to address this issue. High-speed domino logic [27] and conditional keeper are among the most effective solutions for improving the robustness of domino logic. Fig.2.17. the main sources of noise in domino logic circuit [26]. In this section, we propose new domino circuits for high fan-in and high-speed applications in ultra deep submicron technologies. The proposed circuits employ a footer transistor that is initially OFF in the evaluation phase to reduce leakage and then turned ON to complete the evaluation. In order to avoid the delay penalty due to an initially OFF footer transistor, an extra path for evaluation is provided that is controlled by the output. According to simulations in a predictive 70nm process [29], the proposed circuits increase noise immunity by more than 26X for wide OR gates and shows performance improvement of up to 20% compared to conventional domino logic circuits. The proposed circuits reduce the contention between keeper transistor and NMOS evaluation transistors at the beginning of evaluation phase.

An input switching high in evaluation phase:

The waveforms of the circuit in this mode are shown in Fig.3. As observed, the increased voltage of N_FOOT node at the beginning of the evaluation phase causes MP3 to be turned on. Therefore, the GMN2 node is charged to the voltage of N_FOOT node which rises above the threshold voltage of MN2. Therefore, the NMOS transistor MN2 is turned on at the onset of evaluation phase (when the footer transistor MN1 is off), connecting the dynamic node to ground. After delay of the delay element, N_FOOT node is strongly at zero voltage. Thus, the transistor MP3 switches to the off state. Since the output nod is at
 high now, it turns on the MN3, and connects GMN2 node to ground turning MN2 off.
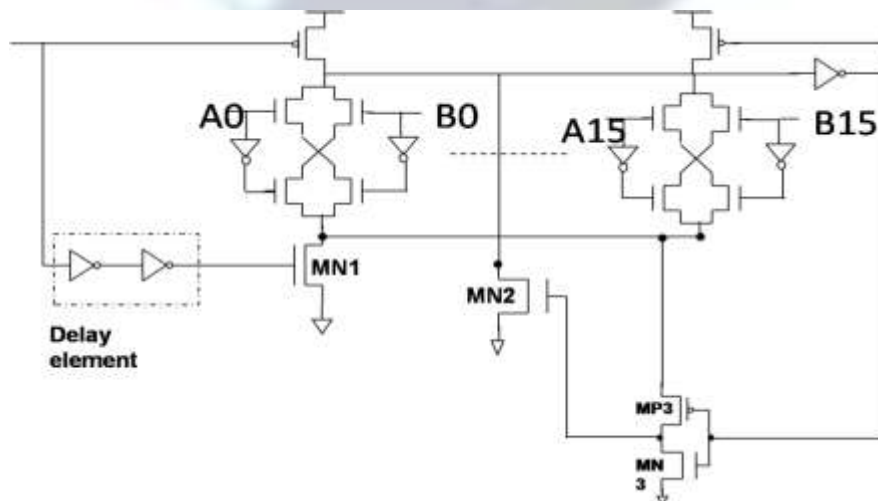
Fig. 3. Proposed comparator-1

However, the rest of evaluation phase (discharging of the dynamic node) completes through the evaluation network and the footer transistor that is fully on. Here we have more degree of freedom for increasing speed or enhancing noise immunity. For example, for improving speed, upsizing of MP3, MN2, MN1, evaluation transistors, and MN1 are all options.

FINFET Circuit Design

Until now we explained different challenges in nano-scale CMOS design especially for low voltage design. However due to significant amount of process variations in nano-scale CMOS technology, considering other devices for low power, high-performance and robust design is important. Aggressive device scaling has led to statistical variability and increased short channel effects (SCE) [141], [142]. Thinner gate oxide helps to improve the short channel effect. However, thinner gate oxide to improve SCE is not a viable option in nanometer scale nodes as it increases the gate leakage exponentially. Hence, a well-defined device should have a good compromise between speed and leakage power. Using high-k dielectric oxide, the total gate capacitance of device is reduced due to the spatial redistribution of electric field. However, using high-k dielectric at the same oxide thickness value degrades both Ioff and Ion compared to using SiO2 [154]. Upsizing the FinFET by increasing the fin width, improves the ON current, while off current is degraded. For FinFET devices, to increase the current more, increasing the number of fins is an approach. However, optimizing the fin pitch to achieve better electrostatics is important. For instance, at iso-fin width, by increasing the fin pitch by 4 times, total gate capacitance is increased by 50% [160]. Another technique to increase Ion current with no penalty on off current is using high-k spacer. This is achieved by some amount of inversion takes place in the underlap region and also because of the encroachment of the fringe fields from the gate through the high $-\kappa$ dielectric. The coupling of the gate fringe field with the underlap region becomes stronger with increasing dielectric constant. Also, the off current is found to decrease at higher values of spacer κ. Hence, using high-k spacer seems to a promising technique to increase the Ion/Ioff ratio [164]. However, gate leakage is degraded by using this technique. Other techniques are source/drain extension and metal gate work function engineering. Hence, using a well-defined device structure for low leakage and robust design is extremely important. The effect of leakage current is more pronounced in SRAMs. Furthermore, Vth variations due to Random dopant fluctuations (RDF) in sub-45nm standard CMOS devices can be one of the major bottlenecks in high density SRAM design. A high threshold voltage variability compromises SRAM cell stability. Due to the large number of transistors in an array, process variations become more significant, thereby different failures are introduced (such as read, write, and access. Furthermore, due to the increased leakage power in SRAM arrays, the introduction of new devices with lower leakage current with improved read and write margins is desired.

Conclusions

In this work, the author has proposed a design methodology for FINFET devices to achieve improved SRAM cells. Specifically, controlling asymmetrically the doping concentration of source and drain contacts we achieve appropriate transistor properties that are used to improve performance of the SRAM cells. The AD-FINFET replaces the access transistors of a conventional SRAM cell and hence it improves concurrently both read and write SNM. Finally with this technique author have achieved at least 20% read SNM and 9% write SNM. In addition our simulation results show 56% reduced access time compared to conventional FINFET SRAM cell.

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