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Static modeling of fully-printed OTFTs using a modified Amorphous-Si: H TFT model

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ABSTRACT

The presented work contributes on the modeling of low cost fully-printed Organic Thin Film Transistors (OTFTs). Due to the lack of OTFTs' models included in industrial and commercial Computer Aided Design (CAD) tools, the Amorphous-Si: H TFT model presents in most CAD tools and initially planned for Amorphous Silicium Hydrogenated Thin Film Transistors (A-Si: H TFTs) was used. In the paper, the parameter-extraction procedure was done using a specific approach based on an iterative method which improves processing time and precision. This allows taking into account the series resistance of the designed OTFTs generally neglected for A-Si: H TFTs. In addition, some parameters appeared to be dependent on the OTFTs' geometry. These geometry dependences allowed the setting up and the creation of a single model valid for a wide range of geometries. The proposed model offers a possibility to design rapidly complex system with more than one hundred OTFTs on flexible plastic foils. It passed all stages of validations in static, and the measurements of some basic circuits were compared with simulation results.

Keywords: A-Si: H TFT, modeling, OTFTs, iterative extraction, geometry dependence.

1. INTRODUCTION

Organic electronics is currently the subject of intense research for several reasons. It is based on materials called conductive polymers or small molecules which require low-cost manufacturing processes and no huge-controlled environment. These low temperature techniques present the advantage of being compatible with flexible substrates like plastics or papers. Due to these advantages, the use of organic electronics is interesting in many applications like for OTFTs manufacturing [1], OLED or solar cells [2] fabrication. Even if the performances of organic components do not match those of inorganic ones,—generally due to the weak mobilities [3], [4] or the high series resistance [5]–[7] — many works recently reported show that some basic [8]–[12] or complex [13]–[15] circuits can be designed. However, to exploit all the possibilities of organic devices and to test their limits, precise models should be available, this will help to predict behavior of the designed circuits.
Although the modeling of OTFTs has been the focus of many papers, most of the proposed models are not scalable [3], [6], [16], and do not include either all stages of model validations [6] or series resistance extractions [17], [18]. In this paper, the Amorphous-Si: H TFT model developed at Rensselaer Polytechnic Institute (RPI) is used. It is present in all modern simulators and allows simulation of complex circuits rapidly. However, the physical phenomena in organic devices are not entirely similar to the ones in amorphous devices then the Amorphous-Si: H TFT model cannot be applied directly to OTFTs and needs modification to integrate the specific geometry dependences of OTFTs parameters. Moreover, the series resistance generally neglected for A-Si: H TFTs should be taken into account in case of OTFTs. The thus-modified Amorphous-Si: H TFT model considering theses dependences proved performant for a large range of geometries.
The paper is divided into six sections. Section 2 is about the OTFT modeling in above-threshold regime and briefly presents the extraction methods. Section 3 presents the iterative extraction procedure applied to OTFTs. In Section 4, the proposed scalable model based on the geometry dependences of extracted parameters is presented. Section 5 focus on the model validation and the last section, with a benchmarking from literature, concludes the paper and announces future works.

The OTFTs manufacturing in the presented work is as follows: over an insulating Polyethylene Naphtalate (PEN) substrate metalized with a 30nm-thick gold (Au) layer, the drain and source electrodes are created by laser ablation. After this, a 100nm-thick organic semiconductor (OSC) layer is deposited by screen printing. The P- and N-type organic semiconductors used are respectively the Polytriarylamine (PTAA) and the Acene-based-diimide. Then, an 800nm-thick dielectric layer (the fluorine polymer oxide) is also formed by screen printing. Finally, a 5µm-thick Ag layer is deposited to form the gate electrode, and a final annealing at 100°C is achieved. The schematic cross section of the designed OTFTs is presented in Fig.1

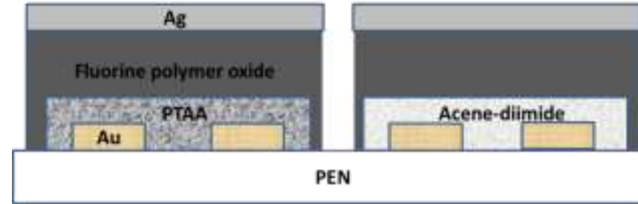

Figure 1. Schematic cross section of the presented OTFTs (top gate/ bottom contact configuration)

2. MODELING IN ABOVE-THRESHOLD REGIME

The UMEM (Unified Model and Extraction Method) approach was used for the parameter extraction. This method allowed the individually extraction of each parameter following a specific order. The main parameters were extracted from the OTFTs' transfer and output characteristics, using the same extraction procedure as in [19], [20] applied on A-Si: H TFTs. Thus, the parameters Gamma (γ), the threshold voltage (V_T), the band mobility (μ_0), the characteristic field voltage (V_{aa}) and the series resistance (R) were extracted in linear regime (low drain-source voltage) using the H function defined in (3). And, the saturation parameters like the saturation modulation parameter (α_{sat}), the channel-length modulation (λ_{sat}) and the knee-parameter (M) were extracted in saturation regime (high drain-source voltage). In linear regime, the current could have been approximated following (1) where W and L are the OTFT dimensions, then, the H function could be rewritten following (4).

$$I_{dslin} = \frac{K*\mu_0*\left(V_{gs}-V_T\right)^{1+\gamma}}{V_{aa}{}^{\gamma}+R*\mu_0*K*\left(V_{gs}-V_T\right)^{1+\gamma}}*V_{ds} \quad (1)$$

$$K = \frac{C_{ox}*W}{L} \quad (2)$$

$$H(V_{gs}) = \frac{\int_0^{Vgs} I_{ds}(x)dx}{I_{ds}(V_{gs})} \quad (3)$$

$$H(V_{gs}) = \frac{1}{\gamma+2}*(V_{gs}-V_T+R*I_{dslin}) \quad (4)$$

The mobility model is expressed in (5). Equation (1) associated to (5) allow rewriting the mobility in linear regime following (6).

$$\mu_{fet}(V_{gs}) = \mu_0*\left(\frac{V_{gs}-V_T}{V_{aa}}\right)^{\gamma} \quad (5)$$

$$\mu_{fet}(V_{gs}) = \frac{I_{dslin}}{K*(V_{gs}-V_T)(V_{ds}-R*I_{dslin})} \quad (6)$$

3. OTFT-SPECIFIC EXTRACTION

A. Discussion about series resistance

In case of A-Si: H TFTs, the threshold voltage is extracted by only considering the intercept of the H function because the term $R*I_{dslin}$ is considered negligible compared with V_T [18],[20]. With the presented OTFTs, the mean value of the ratio $V_T/R*I_{dslin}$ on a sample of 144 N-OTFTs was 27 as shown on the statistical graph in Fig.2 meaning that the term $R*I_{dslin}$ is only 3.7% (1/27) of V_T. This result shows that the term $R*I_{dslin}$ could be neglected in the calculation of the H function, but, it will be shown in the following sub-section that the series resistance could not be neglected during the parameter extraction procedure. The series resistance were calculated using (7) deduced from (1).

$$R = \frac{V_{ds}}{I_{dslin}} - \frac{V_{aa}{}^{\gamma}}{K*\mu_0*(V_{gs}-V_T)^{1+\gamma}} \quad (7)$$

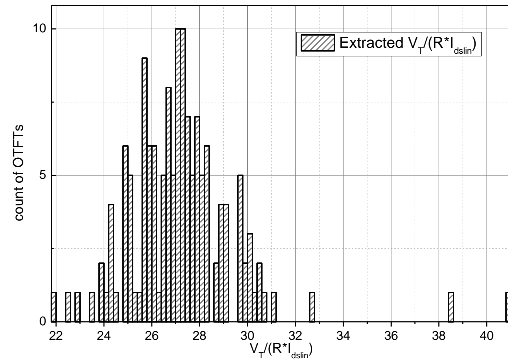

Figure 2. Dispersion of extracted $V_T/R*I_{dslin}$ ratio on a sample of 144 Acene-based diimide N-OTFTs

B. Iterative method for the above-threshold parameters extraction and validation procedure

An iterative method which improves precision and respects the UMEM method was developed as shown in Fig.3. For the extraction method to be valid, reproducibility was tested using different initial values of series resistance, and only a few iterations were necessary to converge to the same value, thus confirming to be independent of the initial value and confirming reproducibility as shown in Fig.4. The iterative extraction method presented in Fig.3 were first applied to one transistor and the results are presented in table 1 showing the impact of series resistance on γ, V_T, μ_0 and V_{aa} parameters.

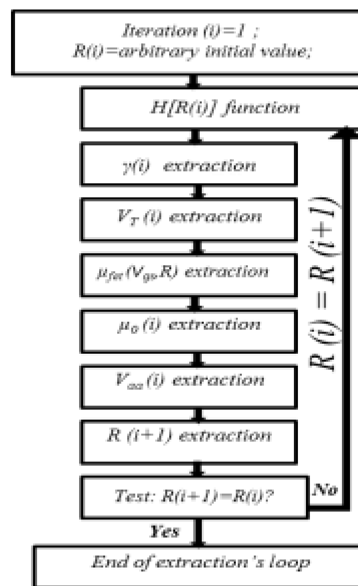

Figure 3. Organization chart of iterative above-threshold parameters extraction

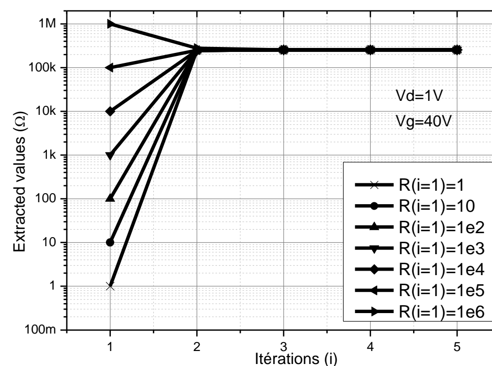

Figure 4. Convergence of extracted series resistance for different initial values, Acene-based diimide N-OTFT, W/L=50, T=25°C

Table 1: Extracted above-threshold parameters for an Acene-based diimide N-OTFT, W/L=1000µm/20µm, (T=25°C).

Parameters	Neglecting R	Considering R
Itérations	1	4
γ	1.64	2.16
VT	4.64	4.45
µ0 (cm²/V.s)	0.32	1.1
Vaa(V)	27	56
R (kΩ)	0	256
αsat	0.16	0.16
λsat (1/V)	0.00176	0.0017
M	2.25	2.25

C. Complete model for all regimess

Although in similar works, recent methods of modeling the sub-threshold and leakage regimes [21], [22] was proved to be very efficient for OTFTs, here, the modeling of the sub-threshold- and leakage-regimes was done using the same expression than in Amorphous-Si: H TFT model by extracting V_{dsl}, E_l ,I_{ol} V_{gsl}, δ_0, V_{min} and Delta parameters. The parameters related on table 1 (considering R) were thus associated to these parameters. Comparisons between modelled and measured characteristics showed correct agreement as shown in Fig.5 and Fig.6. The figures showed also correct agreement in the sub-threshold- and leakage regimes and for the current derivatives (8), (9).

$$G_m = \frac{dI_{ds}}{dV_{gs}} \quad (8)$$

$$G_d = \frac{dI_{ds}}{dV_{ds}} \quad (9)$$

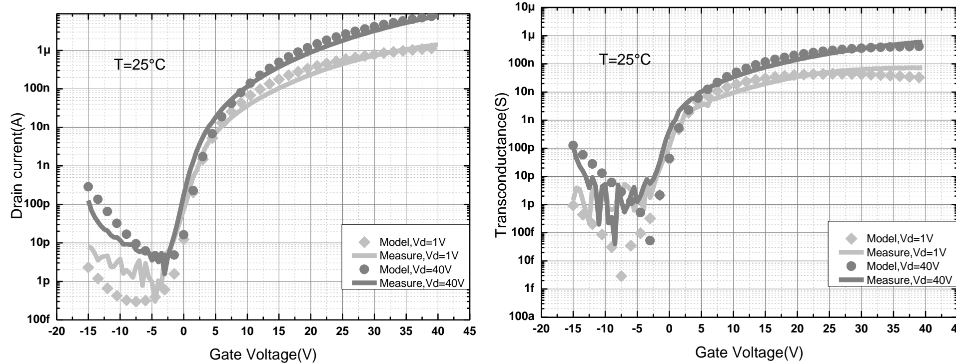

Figure 5. Modelled (dotted) and measured (lines) characteristics (lines) for different V_g bias, W/L=50, Acene-based diimide N-OTFT

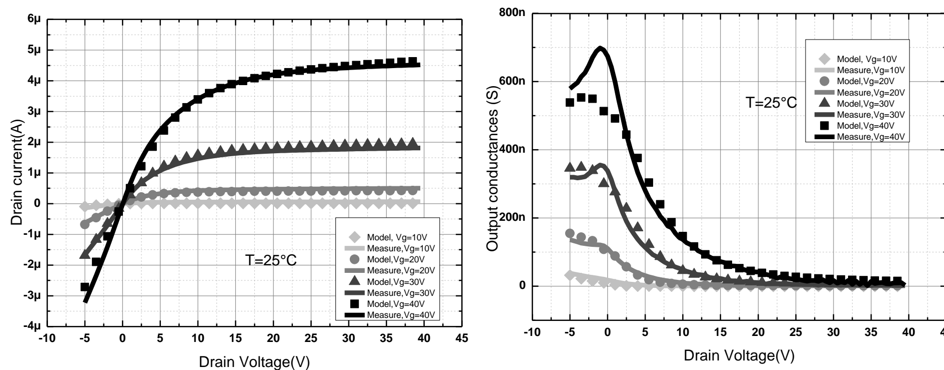

Figure 6. Modelled (dotted) and measured (lines) characteristics for different V_d bias, W/L=50, Acene-based diimide N-OTFT

4. Geometry dependences of extracted parameters

Once the improved extraction procedure validated, the extraction were thus applied to a same sample of 144 N-OTFTs. Only transistors with a same numbers of fingers were studied here. For N-OTFTs having the same dimensions, the extracted values for each parameter were averaged. The objective was to find out whether some parameters are dependent on the OTFT geometry. This was not obvious for small lengths and small W/L ratios, as the process scattering were important for small OTFT sizes and caused a lot of fluctuation, —leading us to consider only W/L ratios between 12,5 and 400. M, V_T and V_{aa} parameters did not appear to be geometry-dependent, thus being considered as process-flow-dependent parameters for which a mean value could be considered for the model. However, others parameters like γ, μ_0, λ_{sat}, α_{sat} and R appear to be geometry-dependent.

D. L-dependence

Reséndiz *et al* [20] tried to find out the effect of length variation on transistor's parameter. He worked on A-Si: H TFTs with channel lengths ranging from 4µm to 12µm. He showed that reducing the transistors' lengths also reduced extracted γ values. Similar results to Reséndiz were found here as shown in Fig.7 and the dependence could be written as follows where γ_0 and B_γ values were extraction-determined constants.

$$\gamma(L) = \gamma_0 * (L)^{B_\gamma} \quad (10)$$

The found dependence of α_{sat} goes in the same way of γ dependence as shown in Fig.7. A physical explication of this result not yet found, further investigation must be done. α_{sat} dependence could be written as follows where α_0 and B_α were extraction-determined constants.

$$\alpha_{sat}(L) = \alpha_0 * (L)^{B_\alpha} \quad (11)$$

For $\lambda_{sat,}$ the extracted values were inversely proportional to length variation following a power law (12) where λ_0 and B_λ are also extraction-determined constants as represented in Fig.7. The found dependence is similar to the same dependence on MOS (Metal Oxide Semiconductor) crystalline transistor: indeed, due to short channel effects changing the physical properties of the transistor, the channel length modulation parameter is higher for short channel-lengths creating higher early voltage. Haddock *et al* [23] found the same progression of λ_{sat} in length variation when studying the short channel effects in OTFTs.

$$\lambda_{sat}(L) = \lambda_0 * (L)^{B_\lambda} \quad (12)$$

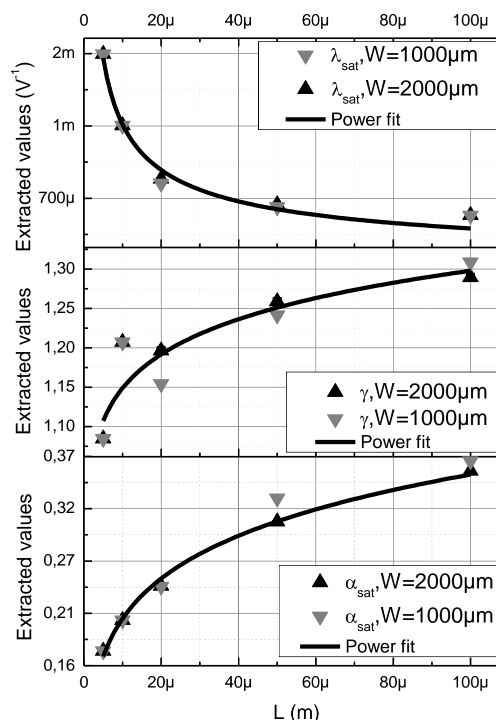

Figure 7. Dependences of extracted $\lambda_{sat,}$ γ and α_{sat} on length variation, Acene-based diimide N-OTFT, T=25°C

E. W/L-dependence

Based on the Amorphous-Si: H TFT model, the W/L ratio is related to the above-threshold current following (13). This dependence initially planned for A-Si: H TFTs was not adequate to the designed OTFTs. To try and understand this phenomenon, we investigated the geometry dependences of R and μ_0, and found a W/L-dependence following (17) and (18) where μ_{scal}, $A_{\mu 0}$, R_{scal} and A_R were extraction-determined constants. These dependences are represented in Fig.8.

$$I_{ds} = \frac{\left(\frac{W}{L}\right) * Cst_1}{1 + \left(\frac{W}{L}\right) * Cst_2} \quad (13)$$

$$Cst_1 = C_{ox} * \mu_{fet}(V_{gs}) * (V_{gs} - V_T) * (1 + \lambda_{sat} * V_{ds}) * V_{ds} * \frac{1}{\left[1 + \left(\frac{V_{ds}}{V_{dsSat}}\right)^M\right]^{1/M}} \quad (14)$$

$$Cst_2 = C_{ox} * R * \mu_{fet}(V_{gs}) * (V_{gs} - V_T) \quad (15)$$

$$V_{dsSat} = \alpha_{sat}(V_{gs} - V_T) \quad (16)$$

$$\mu_0\left(\frac{W}{L}\right) = \mu_{scal} * \left(\frac{W}{L}\right)^{A_{\mu 0}} \quad (17)$$

$$R\left(\frac{W}{L}\right) = R_{scal} * \left(\frac{W}{L}\right)^{A_R} \quad (18)$$

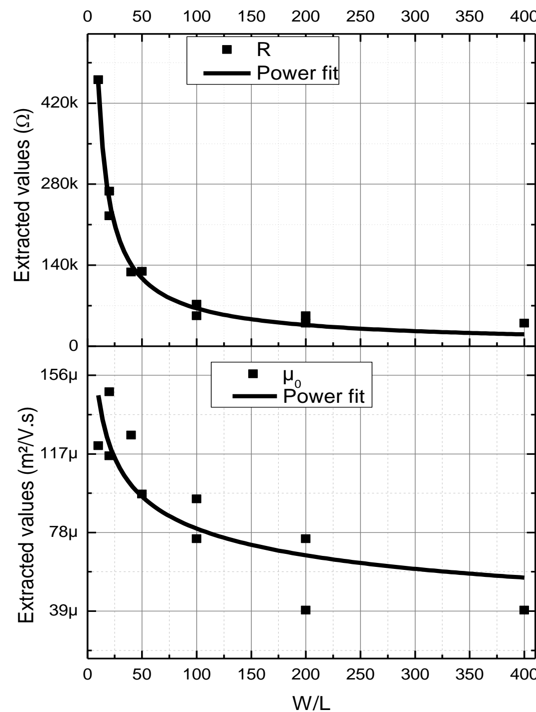

Figure 8. Dependences of extracted μ_0 and R on W/L ratios, Acene-based diimide N-OTFT, T=25°C

Using (5), (10) and (17), the proposed field effect mobility for the OTFTs could then be written as follows.

$$\mu_{fet^{scal}}\left(V_{gs}, L, \frac{W}{L}\right) = \mu_{scal} * \left(\frac{W}{L}\right)^{A_{\mu 0}} * A(L, V_{gs}) \quad (19)$$

$$A(L, V_{gs}) = \left[\frac{V_{gs} - V_T}{V_{aa}}\right]^{\gamma_0 * (L)^{B_\gamma}} \quad (20)$$

In addition, it was found that $A_{\mu 0}$ and A_R have respectively values of -0.46 and -0.58. With these values, the term $R(W/L)*\mu_0(W/L)$ wrote:

$$R\left(\frac{W}{L}\right)*\mu_0\left(\frac{W}{L}\right)=R_{scal}*\mu_{scal}*\left(\frac{W}{L}\right)^{-1,04} \tag{21}$$

Generally, the mobility is intrinsic to the materials and to the device structure. This is the case for MOS crystalline devices, i.e., there is no geometry dependence of the mobility. But for OTFTs, as proved in this work the mobility have a geometry dependence. Indeed, as explained in [24], for higher W, the band mobility decreases due to an increasing number of defects and traps over the larger area within the channel or due to their round geometry which impacts the mobility. In addition, due to the series resistance effects impacting the current for small channel lengths, the band mobility increased with greater L. These two effects help understanding the found dependence of band mobility with small ratios of W/L showing higher mobility. The original Amorphous-Si: H TFT model in above-threshold regime was then modified accordingly, to be usable with OTFTs following (22) and (26).

$$I_{ds}^{'}=\frac{\left(\frac{W}{L}\right)*\left(\frac{W}{L}\right)^{-0.46}Cst_1^{'}(L)}{1+\left(\frac{W}{L}\right)*\left(\frac{W}{L}\right)^{-1.04}*Cst_2^{'}(L)} \tag{22}$$

$$Cst_1^{'}(L)=C_{ox}*\mu_{scal}*A(L,V_{gs})*(1+\lambda_0*(L)^{B_\lambda}*V_{ds})*(V_{gs}-V_T)\frac{V_{ds}}{\left[1+\left(\frac{V_{ds}}{V_{dsSat}^{'}(L)}\right)^M\right]^{1/M}} \tag{23}$$

$$Cst_2^{'}(L)=C_{ox}*\mu_{scal}*R_{scal}*A(L,V_{gs})*(V_{gs}-V_T) \tag{24}$$

$$V_{dsSat}^{'}(L)=\alpha_0*(L)^{B_\alpha}*(V_{gs}-V_T) \tag{25}$$

$$I_{ds}^{'}\approx\sqrt{\frac{W}{L}}*\frac{Cst_1^{'}(L)}{(1+Cst_2^{'}(L))} \tag{26}$$

5. Model validation

Thanks to (26), the currents appeared to present a specific geometry dependence. For the model validation, two steps are presented. Firstly, the measured curves are compared with modelled ones for different geometries. Secondly, the model is tested with basic circuits.

F. Series resistance

In Fig.9, the modelled dependences of series resistance on gate-source voltage for different drain-source voltages are represented. Although in literature, series resistance are L-dependent [25]–[27], the W/L-dependence found here respected the series-resistance dependence on gate-source voltages.

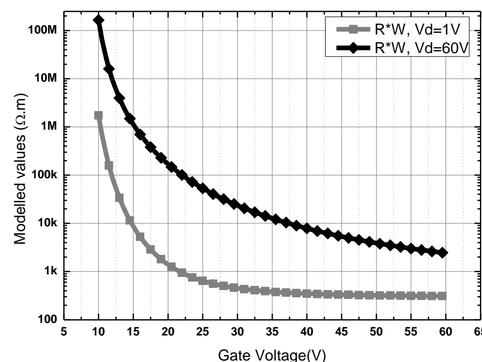

Figure 9. Modelled series resistance of the proposed model, Acene-based diimide N-OTFT, W/L=1000 µm/20µm, T=25°C

G. Model performance

Using the proposed model, modelled curves for different geometries to validate the scalability were compared to measured ones as shown in Fig.10 and in Fig.11.

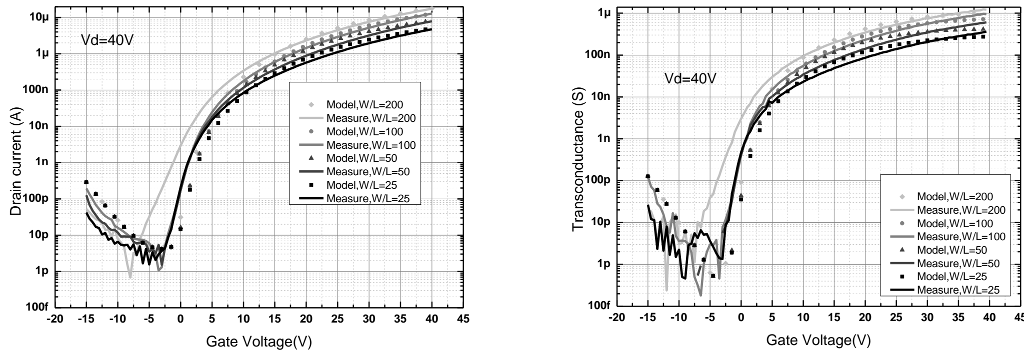

Figure 10. Modelled (dotted) and measured (lines) characteristics for different geometries of Acene-based diimide N-OTFT, Vds=40V, T°=25°C

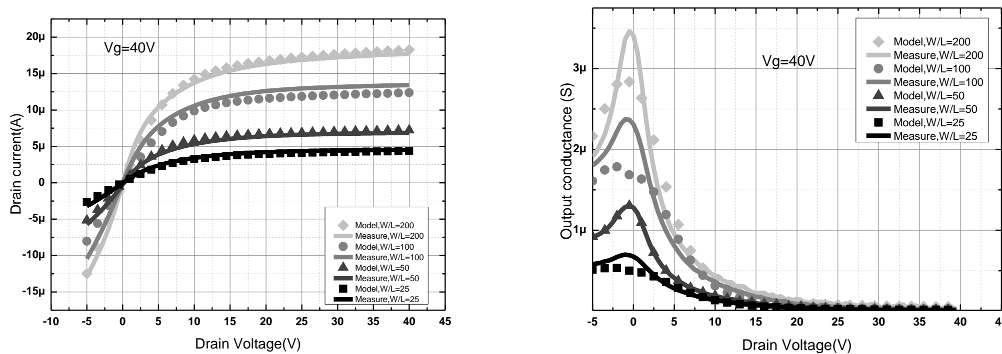

Figure 11. Modelled (dotted) and measured (lines) characteristics for different geometries of Acene-based diimide N-OTFT, Vgs=40V, T°=25°C

The comparison between modelled characteristics and measured ones for different geometries showed correct performance. The presented results for validation were obtained by considering the average measurements of OTFTs with same dimensions. Indeed, there is a non-negligible scattering on the manufacturing process as related in [28].

H. Model test with basic CMOS circuits

The last step validation was to test the model with basic circuits. The model was therefore tested with inverters, NAND and NOR logic circuits. P-type modeling were done separately and independently to the N-Type one but followed the same procedure. Designed organic inverters were made from P-OTFT having dimensions of W/L=25 and N-OTFT having dimensions W/L=50. The schematic and the corresponding picture of one organic inverter are represented in Fig.12. N transistors were twice as big as P one to compensate the mobility difference between holes and electrons. Indeed, extracted mobilities were twice as high for the holes as for the electrons. The compensation permitted to equilibrate inverter with nearly no offset. A high DC gain of 18 both for measurement and simulation was found under a +/- 20V supply as shown in Fig. 13.

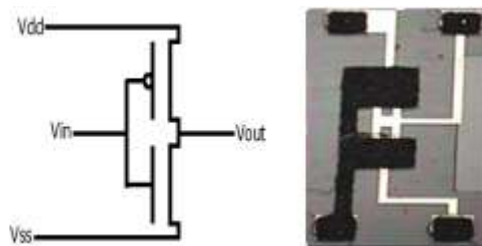

Figure 12. Schematic and picture of a designed organic inverter

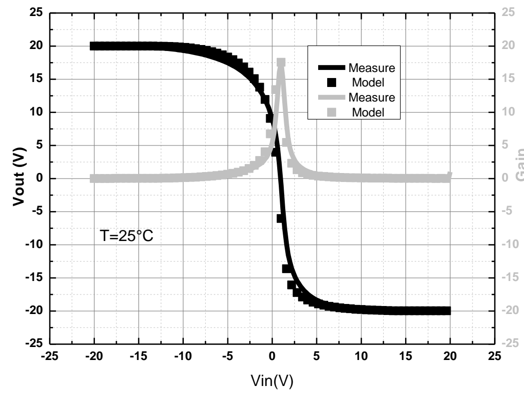

Figure 13. Modelled and measured performances of one designed 1-2 organic inverter

After a validation with a two-transistor circuit, the model was tested with NAND and NOR circuits as represented in Fig.14. Only the inverter function was checked. The circuits were made with N-and P-OTFTs having the same W/L ratios of 50. This, caused an offset to the right due the difference between N- and P-type mobilities. This offset was taken into account by the proposed model as observed in Fig.15.

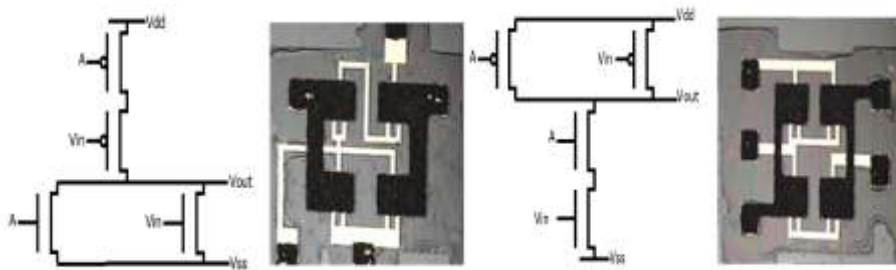

Figure 14. Schematics and pictures of a designed organic NOR (left) and a designed organic NAND (right)

Figure 15 showed that the model was able to predict offsets and gain values found in measurements both for NOR and NAND circuits confirming the correct performance of the proposed model**.**

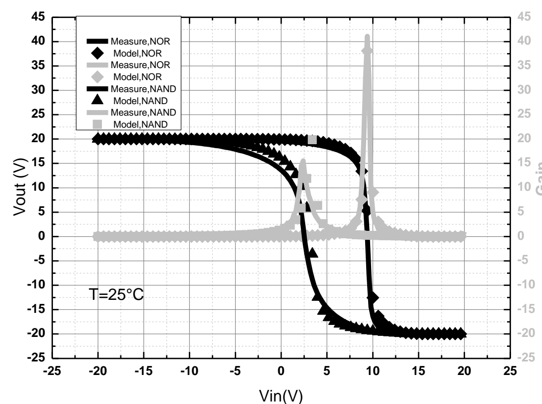

Figure 15. Modelled and measured performances of a designed organic NAND and a designed organic NOR

6. CONCLUSION

This work shows once again the possible use of Amorphous-Si: H TFT model for OTFTs modeling. The new contribution of this work is the improved extraction method applicable to any OTFTs without regards to the geometries, materials or manufacturing process. Another contribution is the geometry dependences of extracted parameters, at the same time permitting to adapt the original model for OTFTs and allowing the creation of a single model for different geometries. Table 2 summarizes the model performance and shows the effort done in series-resistance modeling and in circuit validations compared with others works. At the moment, the presented model includes the static part at ambient temperature. In future works, temperature and dynamic parts will be inserted.

Table 2: Benchmarking of the proposed model with literature

	[17]	[29]	[This work]
Model card(s)	Several	Several	Single
Current derivatives validations	No	No	Included
Validation with basic circuits	No	Included	Included
Series resistance modeling	No	Included	Included
Model	A-Si: H TFT	VRH	Modified A-Si: H TFT

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