International Journal of Enhanced Research in Science, Technology & Engineering
ISSN: 2319-7463, Vol. 4 Issue 10, October -2015

# Embedded Servomotor Control Based on RIO Architecture

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**ABSTRACT**

**Hardware-Description-Language (HDL) is deployed in digital hardware implementation of the control systems. A deep knowledge in digital hardware design is essential for successful implementation. To cope with this concern in mind, there is a great interest to employee alternative tools to rapidly implement the developed control algorithms. This will effectively simplified and shorten the time for innovation. For this reason, this paper aims to demonstrate the methodology of using the new LABVIEW-FPGA tool in rapid embedded system design of digital control algorithms. Here, a well-known digital PID filter to track the position of the servomechanism system is implemented. Single RIO (9636) platform from National Instrument (NI) and the prototyped position control system (33-100 & 33-110) from feedback device are adopted for embedded control design. Experimental test confirm the successful hardware implementation of the control algorithm. Results shows that the digital PID controller uses only 625 slices, 1697 register, 1438 LUTs, and it can be operated with very high sampling rate.**

**Keywords: LABVIEW-FPGA, Rapid hardware implementation, Position control, FPGA, Digital PID controller.**

## 1. INTRODUCTION

It is well known that Hardware Description Language (HDL) is typically used in embedded control system based on FPGAs. This design process can be accomplished by successful development of thousands of text line code; therefore an expertise in embedded architecture design is essential for efficient hardware implementation. From the industry point of view, this will increase the time to the market or the development cycle as well as the development cost [1]. On the other side, this knowledge on the architecture design is unnecessary for the developer of control system. From this prospective, there is increase popularity to employee an alternative modern development environment for rapid hardware implementation based FPGAs. As an illustrative example, Xilinx system generator Simulink by MATLAB environment and LABVIEW-FPGA module by National Instruments based LABVIEW environment. These two high level languages provide the opportunity to easily and quickly develop the highly complex algorithms without or with little committing to hardware design [2]. Therefore, the trend now is to endorse these tools to be competitive as compared with text based languages in term of performance and hardware resources [3]. It has been noticed that the advance development in LABVIEW-FPGA promoted the researcher and engineers to utilize the facility and tools that offer by LABVIW-FPGA [4]. This can be found in recent research presents in [3-9]. In spite of simplicity and hardware compatibility that provided

by the LABVIEW-FPGA, but the work in this field is progressing slowly. Therefore, this paper illustrates the effectiveness and methodology of using LABVIEW-FPGA tool in embedded control systems. Here, the embedded control design of the servomechanism system is considered; however the developed procedure can be easily applied to the other control system. This paper is organized as follows: the development flow of the LABVIEW-FPGA and RIO configuration is presented in section 2, while section 3 demonstrates the experimental validation of the hardware implementation. Finally, conclusion is presented in section 4.

## 2. RIO Configuration and LABVIEW-FPGA Development Flow

This section describes the hardware architecture of the NI-Single RIO embedded control board. As shows in Fig.1, the single board RIO hardware architecture is integrated both the reconfigurable FPGA chip and the real time processor. As well as, the analog and digital input / out ports are directly connected through the buses with the FPGA chip [11]. This making the FPGA chip working as an intermediate process that linked the low level hardware resource with the high level real time processor. The combination between the FPGA device and the real time processor is done via high speed duplex PCI bus. Importantly, similar hardware architecture is shared between the single RIO board and the Compact RIO platform [11].

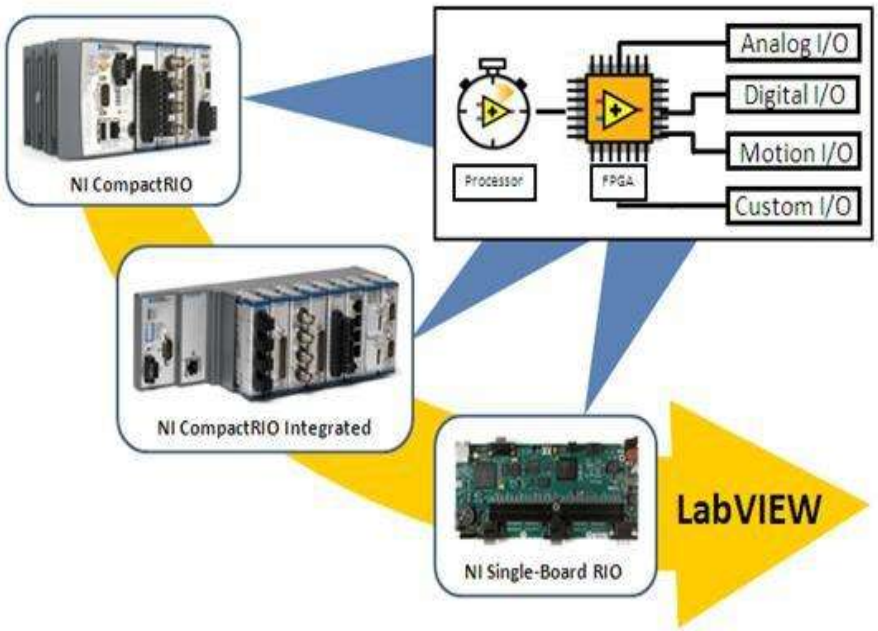



**Figure 1: Generic RIO architecture [12]**

In order to pass the data for real time processing (ie. data monitoring, data logging, …) as well as passing the data from the FPGA to the real time processor or from the I/O ports and the FPGA; a data-transfer mechanisms is provided by the LABVIEW-FPGA tools. In this work the SbRIO-9636 system is used. The features of this board are as follow: Spartan-6 size LX45 reconfigurable FPGA manufactured by Xilinx, real time processor with 400 MHz industrial processor with 512 MB nonvolatile storage and 256 MB DRAM for deterministic control and analysis, different hardware resource are also available: 16 channels of 16-bit analog inputs (A/D), ± 10V, 4 channels of 16-bit analog outputs (D/A), ± 10V, 28 pin of DIO lines, integrated 10/100BASE-T Ethernet, RS232 serial, RS485 serial, USB, CAN, and SDHC ports [13]. The attached daughter card with the SbRIO-9636 is also offered to the designer a selection of mounted I/O ports including temperature sensor, variable potentiometer, LCD Function generator, LED, and push button switch.

To make the hardware implementation more manageable, it is essential to develop a systematic approach that can be followed in the design process. Fig.2 (a), shows that there are several steps to develop the hardware implementation using LABVIEW-FPGA tool [10]. Fig.2 (b, c), shows that there are two modes of operation: host interactive mode and interactive mode [3]; in this work an interactive mode is utilized, more details can be found in [3].

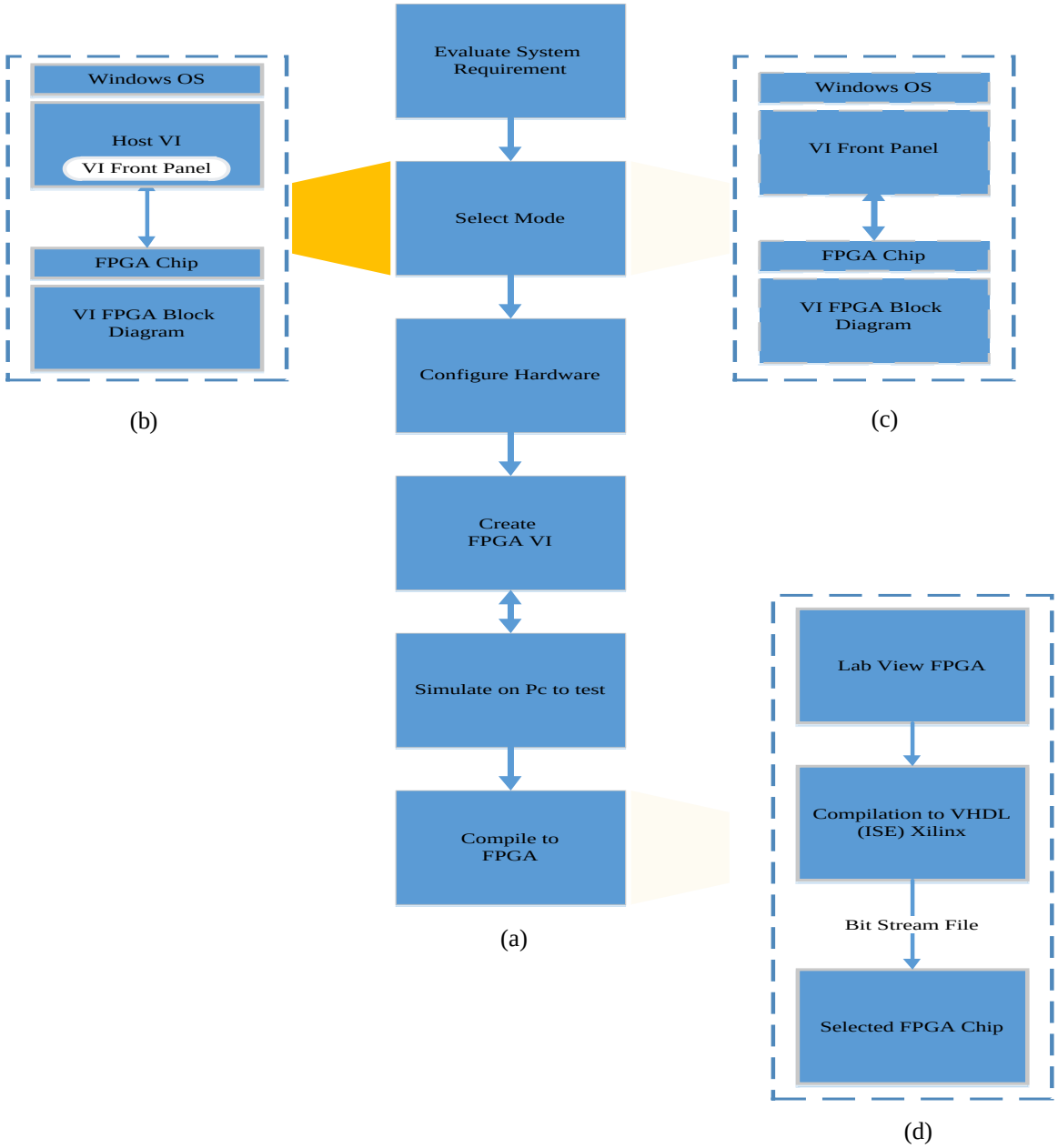



**Figure 2: a- LABVIEW –FPGA development flow, b- Host interactive mode,**

**c- Interactive mode, d- Compilation process [3]**

## 3. System Configuration and Experiential Results

The development flow presented in section 2 is employed for real time implementation of the control system. Fig.3 show the closed loop control system and Fig.4 depict the system setup for real time control of the servomotor system. The implementation of the control system is divided into two levels (Hardware level and software level). The hardware level composes of two platforms. The first platform is the RIO board which is directly connected to the second prototype system (33-100&33-110/Servo Motor module), to acquire the input/output signals. Interactive mode is utilized for real time embedded control design. This means that all the functions are executed by the RIO device. Firstly, acquiring the sensed position signal by the dedicated A/D converter and then pass the converted signal to the designed digital PID filter, finally send the generated control action signal to the process unit via the plugin D/A converter. Again, the procedure of implementation is divided into two phases: develop the code in host PC and then

controlling it by the FPGA. However, for complex and advanced control system, host-interactive mode is preferable. This mode allows the designer to use all the available resources of the RIO platform. Equation (1) described the implemented digital PID filter and the schematic diagram is shown in Fig. 5. The schematic diagram is then transfer into a wire connection for real hardware implementation (see Fig. 6). From Fig. 6, it can be noticed that the digital PID filter is coded using the high throughput block sets, this will plainly reduce the hardware utilization.

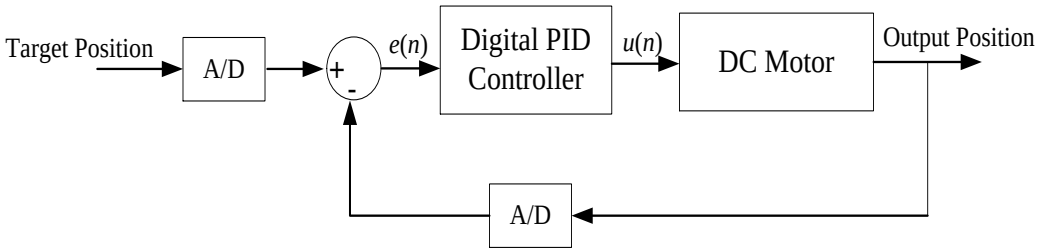



**Figure 3: Closed loop control of DC motor system**

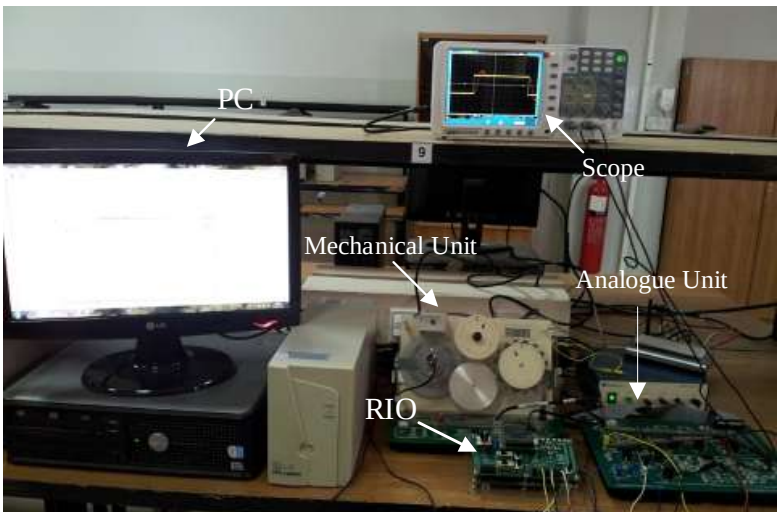



**Figure 4: Experimental hardware prototype system setup**

$$C_{PID}(z) = \frac{U(z)}{E(z)} = K_p + K_I \frac{z}{z-1} + K_D \frac{z-1}{z-\alpha} \quad (1)$$

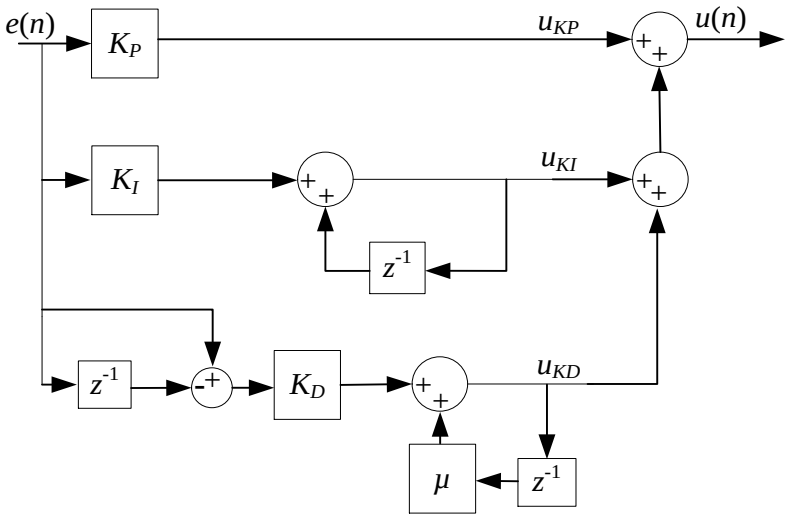



**Figure 5: Schematic of digital PID controller**

Note that the parameters of the DC motor are completely unknown (unknown model), thus a trial and error approach is adopted in this experiment to determine the suitable PID gains. However, model estimation techniques can be used to find the transfer function of the system. This will ultimately improve the dynamic performance of the closed loop system. This point can be considered in future work. Now, in order to validate the hardware implementation of the implemented PID controller as well as to test the overall dynamic response, the reference signal; here the desired position signal is changing abruptly to different position values. Fig. 7(a & b) present the dynamic response of the closed loop system for different position angles (clockwise/anticlockwise). Clearly, the experimental results demonstrated that the designed controller has the ability to track the rapid change in the position signal. Finally, the hardware resources utilization for the developed digital PID controller is presented in Table 1. It is clearly showing that a small amount of resources has been used in this block set (PID).

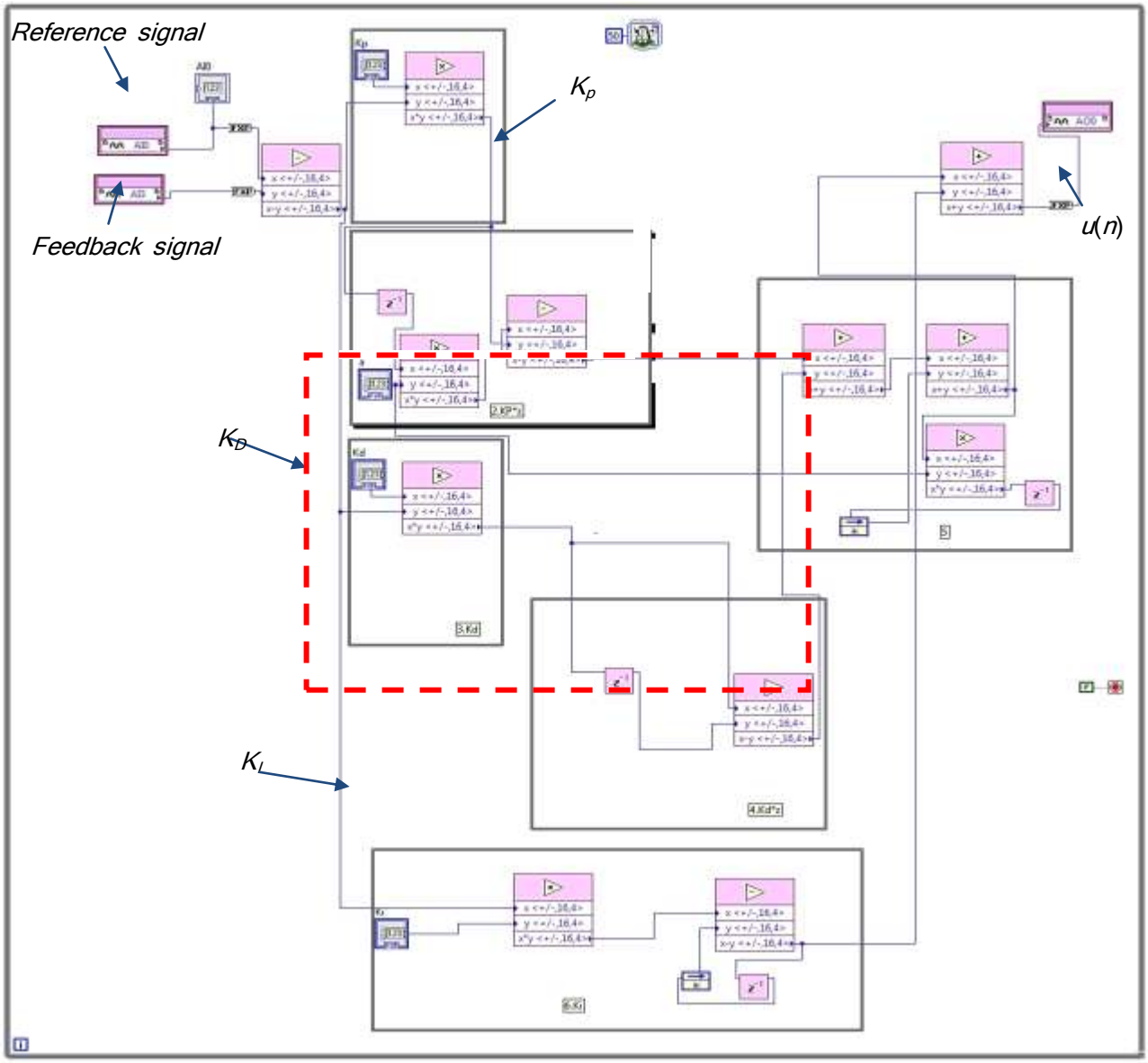
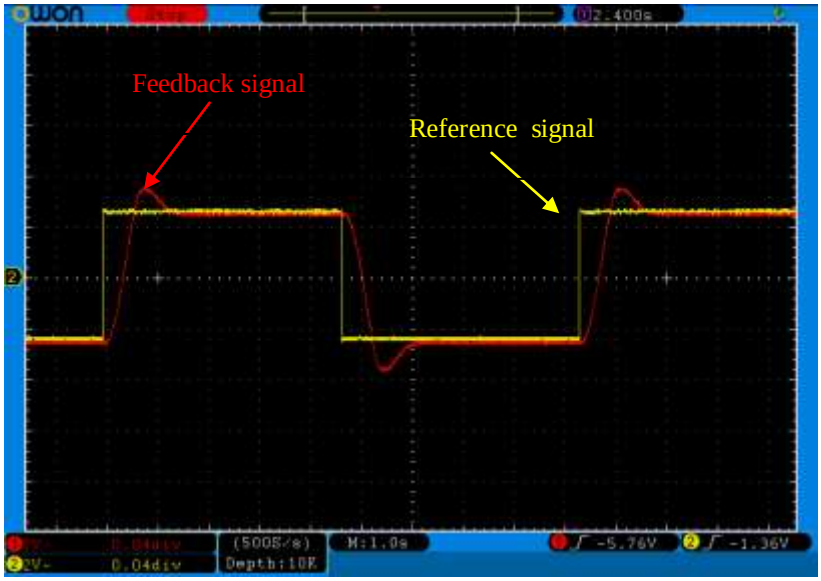
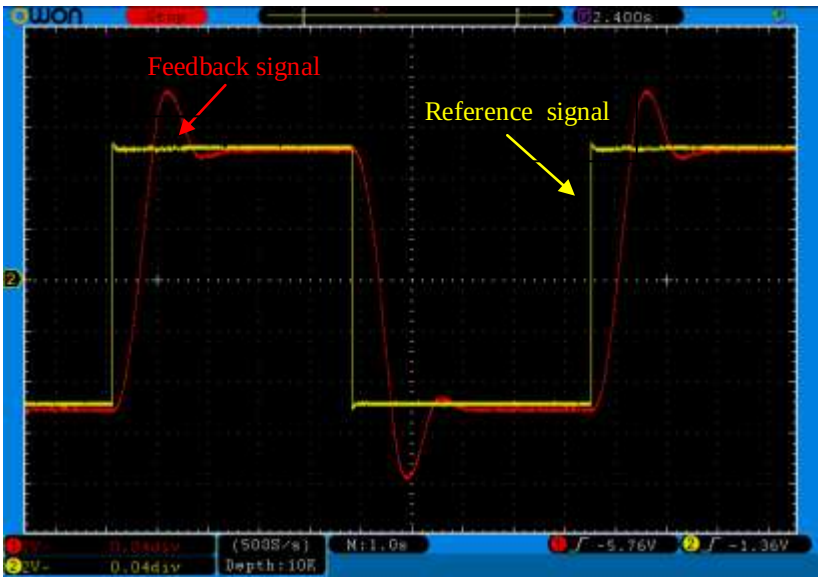



**Figure 6: Wire diagram of the digital PID filter with input/output signals**




(a)




(b)

**Figure 7: Output response to the rapid position change.**

**Table 1: Hardware resources summary**

| Device Utilization | Used | Total | percent |
|---|---|---|---|
| Number of Slices | 625 | 6822 | 9.2 % |
| Number of Slice Registers | 1697 | 54576 | 3.1 % |
| Number of slice LUTs | 1438 | 27288 | 5.3 % |
| Number of DSP48s | 7 | 58 | 12.1 % |

## 4. Conclusion

This paper introduced the rapid hardware implementation of the digital PID controller for servomechanism system. RIO structure based on LABVIEW-FPGA tools is used. It has been concluded that learning the HDL is not necessary for embedded control design. This in turn will eliminate the barrier for rapid hardware implementation and for designing a truly real time control system. Experimental results demonstrated the successful hardware implementation using LABVIEW-FPGA module. Finally, we significantly recommended the use of this technique in rapid learning of embedded system design and for fast testing and implementing the control algorithms.

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