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Simulation of ZVZCS Based DC-DC Boost Converter

Rajesh K[1], M.Suman[2], A. Hanumaiah[3], M V Sudarsan[4],

[1,2,3,4] JNTUK, EEE Department, VLITS, Andhra Pradesh, INDIA

ABSTRACT

This paper presents the design and simulation of the zero voltage zero current switched non isolated dc- dc boost converter. Many applications powered by batteries need high performance, high step up dc-dc converters. When the converter switches are turned on and off at high frequency to meet dynamic and steady state requirements, the losses add on in the converter. When current through the switches is zero switching off and switching on at zero voltage is one possible solution to minimize the switching losses which can be achieved with the help of resonating circuit. With an optimum design of resonating elements, high step up voltage can be obtained. One such approach where an input DC voltage of 70V is boosted to 560V with Zero Voltage and Zero Current Switching (ZVZCS), with reduced switching frequency ZVZCS boost converter is compared with conventional boost converter is presented in this paper. The proposed scheme is verified with the help of simulation results using MATHLAB.

Keywords: High Gain DC chopper, Non-isolated, Soft switched

1. INTRODUCTION

The demand for non-isolated high boost DC to DC converters has been gradually increasing in accordance [1] with the growth in dc backup energy systems for uninterruptible power system (UPS). There are two major concerns related to the efficiency of a high step up dc-dc converter: large input current and high output voltage [3-9]. The large input current results from low input voltage; therefore, low voltage rated devices with low on state resistance are necessary in order to reduce the conduction loss. The boost and buck-boost converters are the simplest non-isolated topologies. The non-isolated converters can provide high step-up voltage gain without extreme duty ratios. Shih-Kuen Changchien and Tsorng-Juu Liang [2] in 2003 proposed a novel high step-up dc-dc converter, which utilizes a voltage doubler and adjusts the turn ratios of the coupled inductor. This converter has been highly efficient because it recyc1es the energy stored in the leakage inductor of the coupled inductor, but Stress across the switches is high and large inductor leakage current may damage the switches. Transformer less DC-DC Converters with High step-up voltage was developed by Gain Lung-Sheng Yang, Tsorng-Juu Liang[11] in 2009. This converter uses two inductors with the same level of inductance are charged in parallel during the switch-on period and are discharged in series during the switch-off period. However this converter uses only one active switch for the energy conversion, which also suffers very high current during the switch-on period.

The converter is suitable for low-to-middle-power applications. Yi-Ping Hsieh and Jiann Fuh Chen in 2011 proposed a converter with high efficiency and high boosting capability [12].High step-up voltage gain and high efficiency was achieved by charging the capacitor in parallel and discharging in a series the coupled inductor. This converter experiences extremely high input current at full load, which would lead to high conduction loss during the switch turn-on period. Another ZVZCS based topology was proposed by Yohan Park, by oungkil Jung, and Sewan Choi in 2012 [9]. This converter shows zero voltage switching turn-on of the switches in continuous conduction mode as weIl as reduced turn off switching losses owing to the switching method that utilizes Ir-er resonance in the auxiliary circuit. Also, as a result of the proposed switching method, the switching losses associated with diode reverse recovery are alleviated even for small duty cyc1e. The capacitance in the auxiliary circuit is significantly reduced compared to the pulse width modulation method. ZCS turn off if main switches is not attained in this topology. A high step up DC-DC converter with optimized parameters is designed which yields better output voltage compared to the converter in [12] with reduced switching frequency and the switching losses. The same is justified with the help of simulation results.
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2. PROPOSED CONVERTER OPERATION

Figure1. Shows the converter topology which has the same topology proposed in [12], but with different design specification. The converter consists of a boost converter as the main circuit and an auxiliary resonant circuit which

inc1udes capacitor Cr ' inductor Lr ' and two diodes D_U and D_L .Two switches S_U and S_L are operated with asymmetrical complementary switching to regulate the output voltage.

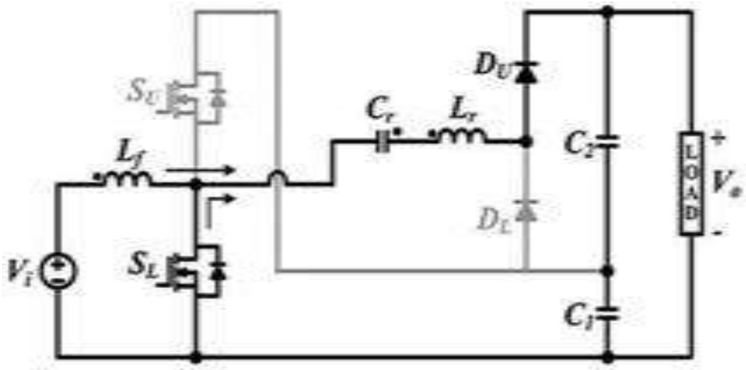


Figure1. High Voltage gain DC-DC boost Converter

The auxiliary circuits not only helps in boosting capability but also ensures ZVS turn on of two switches can naturally be achieved in continuous conduction mode by using energy stored in filter inductor Lf and auxiliary inductor Lr• Unlike PWM method in which the switches are turned OFF with high peak current, the proposed converter utilizes resonance of auxiliary circuit, thereby reducing the turn-off current of switches. Furthermore, for resonance operation, the capacitance of Cr is reduced by a greater value. Various modes of operation are shown in Figure2.

Mode 1 (t_0–t_1): This mode begins when upper switch $S_U$which was carrying the current of difference between i_{Lf} andi_{Lr} is turned OFF. S_LCan be turned ON with ZVS if gate signal for S_L is applied before the current direction of S_L is reversed.Filter inductor currenti_{Lf} and auxiliary currenti_{Lr}starts tolinearly increase and decrease, respectively, as follows

$$i_{Lf}(t) = \frac{Vi}{Lf}(t - t_0) + i_{Lf}\ (t_0)$$
$$i_{Lr}\ (t) = \frac{VCr,min - Vo}{Lr}(t - t_0) + i_{Lr}(t_0)$$

This mode ends when decreasing currenti_{Lr} changes its direction of flow. Then $D_U$is turned OFF under ZCS condition

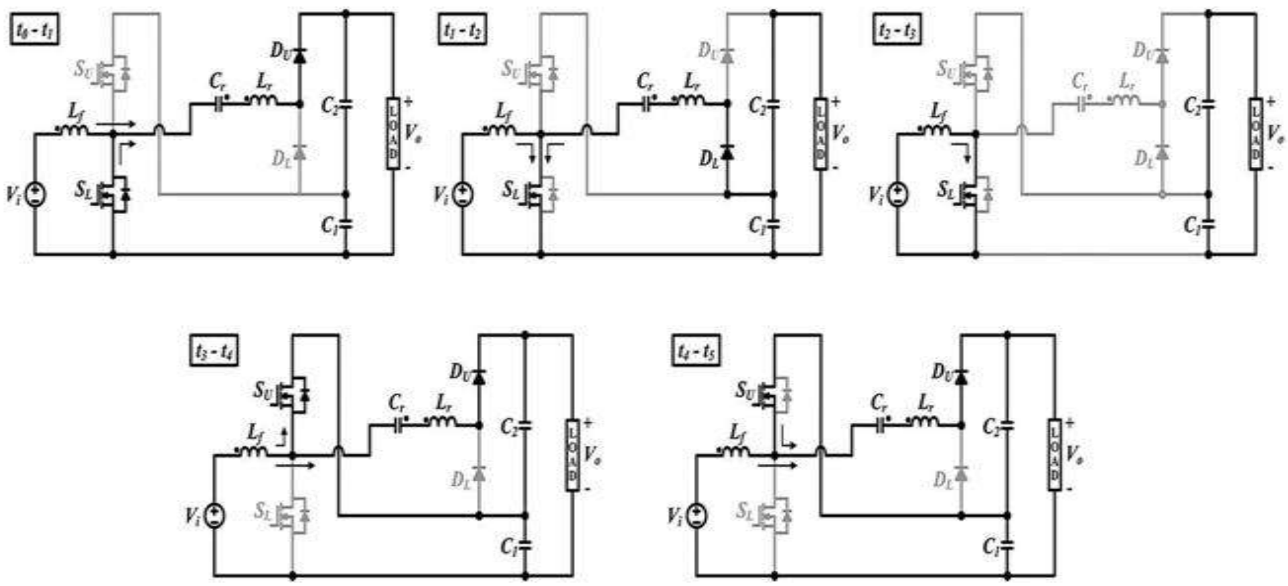


Figure2. Modes of ZVZCS Based DC-DC Boost Converter

Mode 2 (t_1–t_2): This mode begins with L_r–Cr resonance of the auxiliary circuit. Currenti_{Lf} is still linearly increasing. The voltage and current of resonant components are determined, respectively, as follows:

$$i_{Lr}(t) = -i_{Cr}\ (t) = \frac{Vr,2}{Z}\ \sin\left(w_r\ (t - t_1)\right)$$
$$V_{Cr}\ (t) = V_{r,2}\ [\cos\left(w_r(t - t_1)\right) - 1] + V_{Cr}$$

Where$V_{r,2}$ =$V_{Cr,min}$− V_{C1}, Z=$\sqrt{Lr/Cr}$, and w_r=1/$\sqrt{LrCr}$
This resonance mode ends when i_{Lr} reaches to zero. Note that $D_u$is turned OFF Under ZCS condition.

Mode 3 (t_2–t_3): There is no current path through the auxiliary circuit during this mode. Output capacitors supply the load. At the end of this mode the turn-off signal of $S_L$is applied. It is noted that the turn-off current of $S_L I_{SL,off}$ is limited to filter inductor current at t_3, $I_{Lf,max}$ which is much smaller than that of PWM method.

Mode 4 (t_3–t_4): This mode begins when lower switch $S_L$is turned OFF. S_UCan be turned ON with ZVS if gate signal for$S_U$is applied before the current direction of $S_U$is reversed. Filter inductor currenti_{Lf}starts to linearly decrease since voltage v_{Lf}becomes negative

$$i_{Lf}(t) = \frac{Vi-Vc1}{Lf}(t - t_3) + i_{Lf}(t_3)$$

Like Mode 2, the other L_r–Cr resonance of auxiliary circuit is started, and $D_U$starts conducting. Equivalent circuit of resonant mode is shown in Fig. 2. The voltage and current of resonant Components are determined, respectively, as follows:

$$i_{Lr}(t) = -i_{Cr}(t) = \frac{Vr,4}{Z} \sin(w_r(t - t_3))$$
$$V_{Cr}(t) = V_{r,4}[\cos(w_r(t - t_3)) - 1] + V_{Cr}(t3)$$

Where $V_{r,4}$ =$V_{Cr,max}$−V_{C2}, Z=$\sqrt{Lr/Cr}$, and w_r=1/$\sqrt{LrCr}$
This mode ends wheni_{Lr} is equal toi_{Lf}

Mode 5 (t_4–t_5): After i_{Lr} equals i_{Lf}, i_{SU} changes its direction, then this mode begins. At the end of this mode, turn-off Signal of $S_U$is applied and this mode ends.

3. DESIGN SPECIFICATIONS

A. Design of f_r

The resonant frequency $f_r= \frac{1}{2\pi\sqrt{LrCr}}$
Below resonance 2f_r > $\frac{fs}{Deff}$ and above resonance 2f_r < $\frac{fs}{Deff}$
Where f_s is switching frequency, $D_{eff}$is Effective duty ratio and D is duty ratio.

B. Design of Filter Inductance

Considering the input current ripple. I_{in}, input
Filter inductor $L_f$is determined by

$$L_f = \frac{1}{2}\frac{D.Vin}{\Delta Iin.fs}$$
ΔI_{in}= 20% and ΔV_o=5%

C. Design of $L_r$and C_r

$L_r$is determined from the following equations

$$\frac{1}{2}=L_r(IL_r, +pk - IL_r, min)^2 > \frac{1}{2}(C_{OS,L}+C_{OS,U})\left(\frac{1}{1-D}\right)^2$$

Where $C_{OS,L}$ and $C_{OS,U}$ and are the output capacitance of lower and upper switches, respectively.

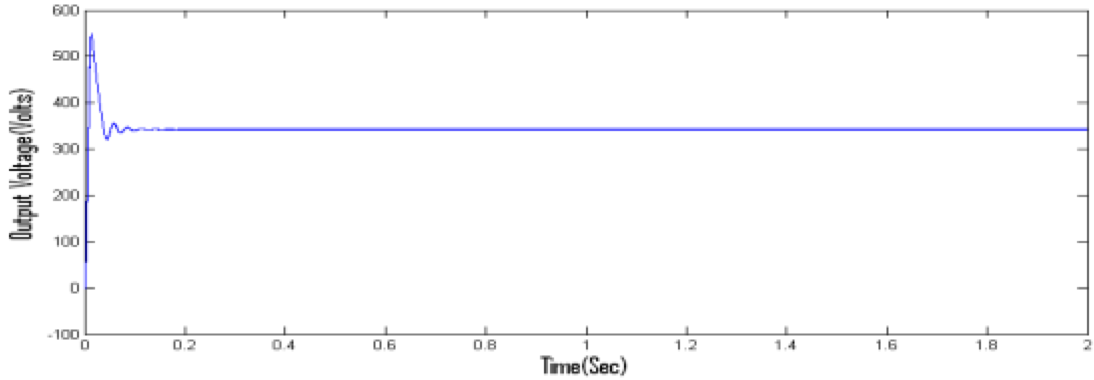
$$\frac{1}{2}=I_{Lf,max} > \frac{1}{2}(C_{OS,L}+C_{OS,U}))\left(\frac{1}{1-D}\right)^2$$

The C_r is given from the equation
$f_r= \frac{1}{2\pi\sqrt{L_rC_r}}$
The designed values are listed in Table 1

4. SIMULATION RESULTS

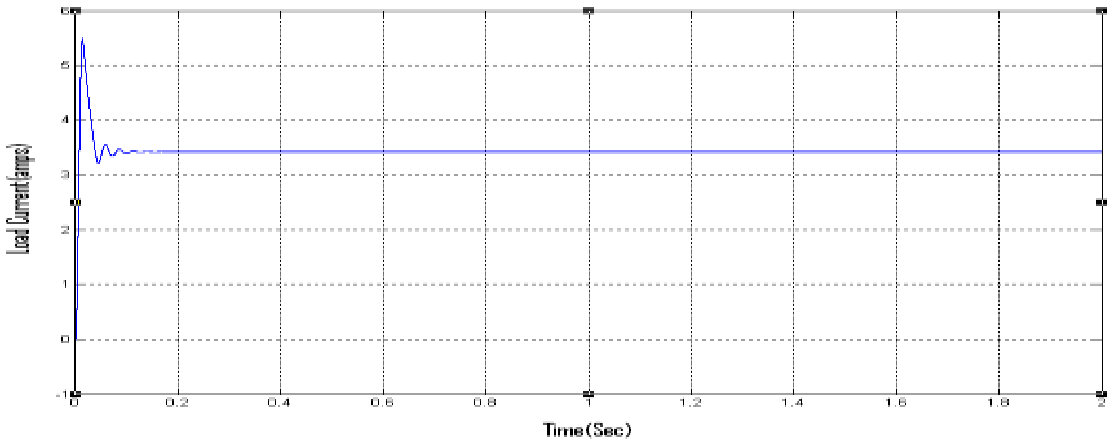
D. Simulation results of boost converter

Graph 1 shows the average DC output voltage response of the boost converter and the converter delivers an average DC voltage of 360 Volts to the load. The output voltage settles to its steady state value of 360Volts at 0.17 Seconds, with considerable oscillations.



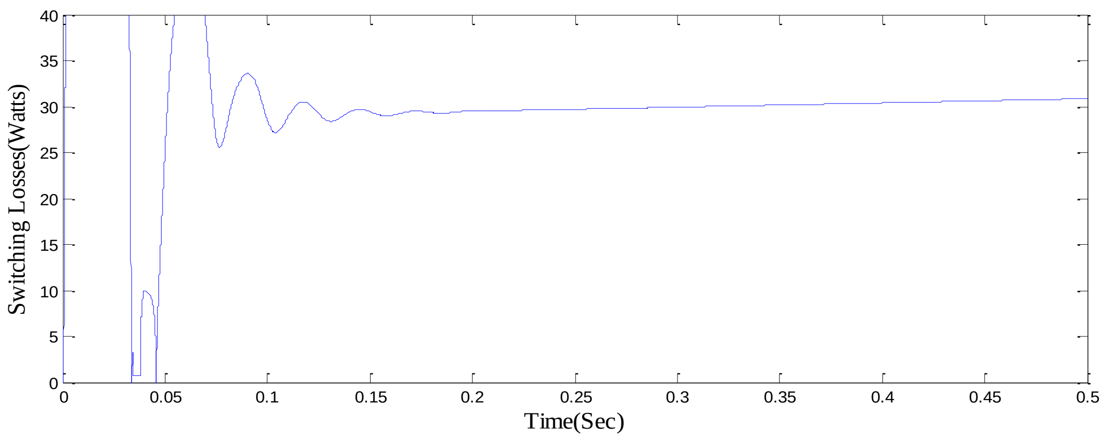
Graph 1.Average output voltage response of boost converter

Graph 2 shows the average DC output current response of the boost converter. The output current settles to its steady state value of at 0.17 Seconds, with considerable oscillations.



Graph 2.Average output current response of boost converter

Graph 3 shows the average power loss across the MOSFET switch during the operation of the boost converter and the converter dissipates an average power loss of 34.52 Watts across the switch. This power loss comprises of both the switching losses and conduction losses together

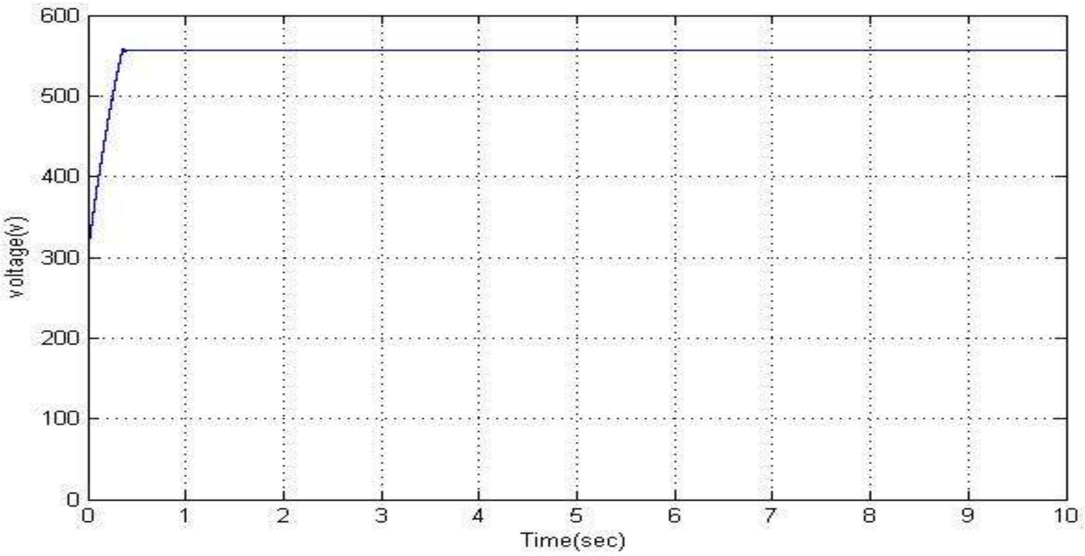


Graph

3.Average power loss across the switch (MOSFET) of boost converter

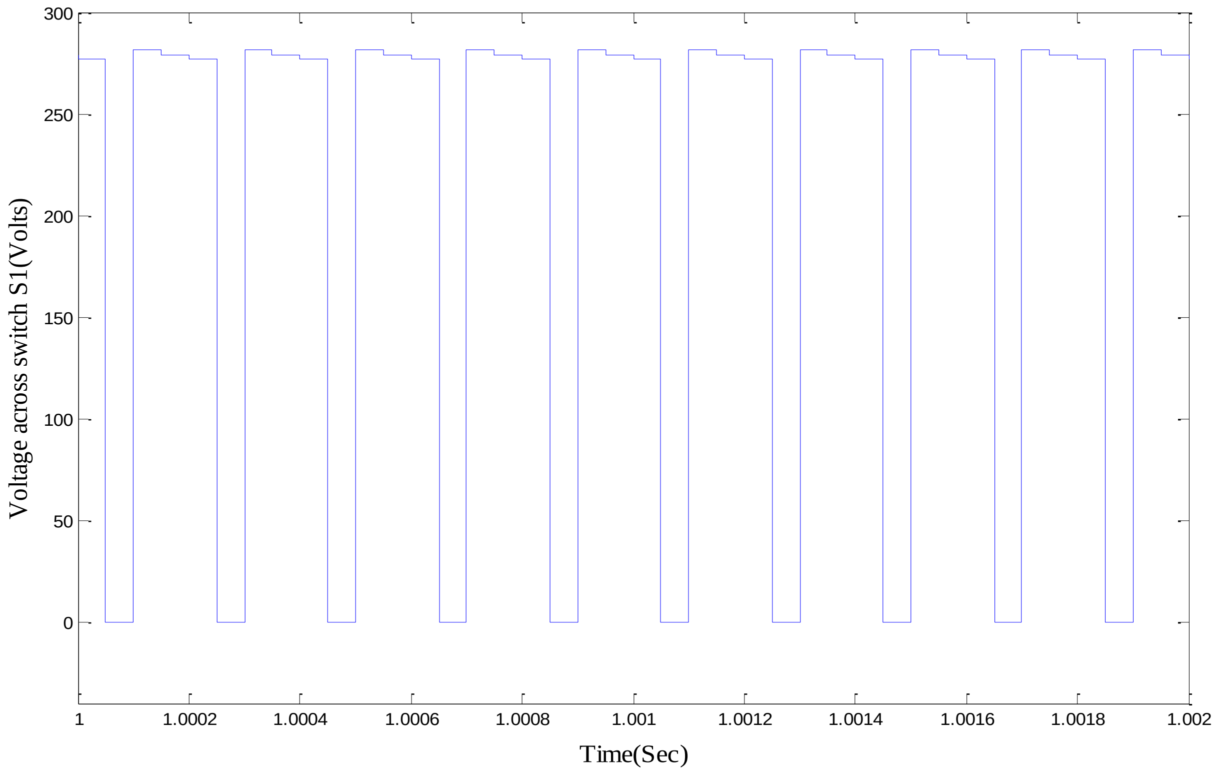
E. Simulation results of ZVZCS Based DC-DC Boost Converters:

Graph 4 shows the average DC output voltage response of the ZVZCS based boost converter and the converter delivers an average DC voltage of 560 Volts to the load. The output voltage settles to its steady state value of 560Volts at 0.0305 Seconds, with negligible oscillations.



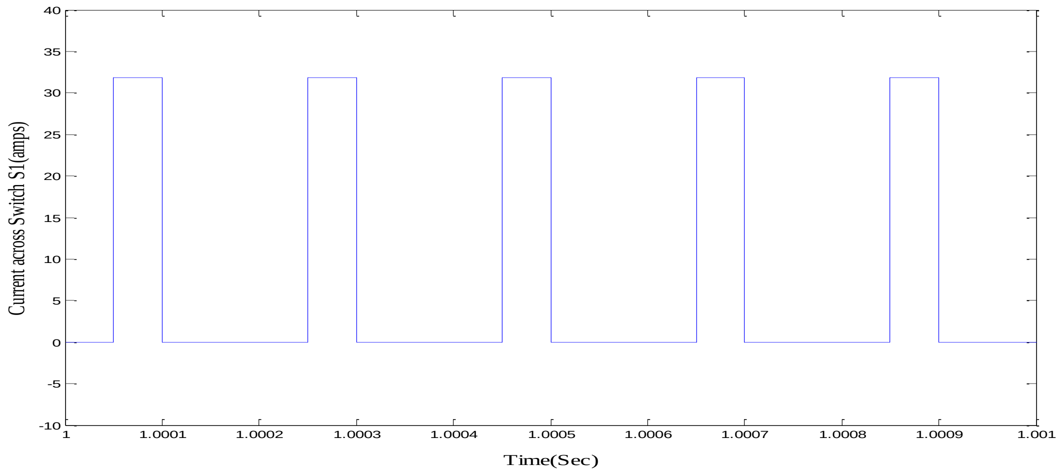
Graph 4.Average Output Voltage response of a ZVZCS Boost Converter

Graph 5 shows Average Output Voltage across the switch (S_U) ZVZCS Based DC-DC boost converter. As observed from Figures 5 and 6 during the rise time of both the switches, the voltage across them is zero, which ensures ZVS turn on of both the switches. During the fall time of switches, the currents I_{s1} and I_{s2} are decayed to zero which implies ZCS turn off of both the switches. Hence ZVS turn on and ZCS turn off of all switches is achieved. As observed from the below simulation results V_{s1} and V_{s2} are equal to 280V. Therefore the stress across the switches during non-conduction period is very much lesser compared to the earlier configurations.



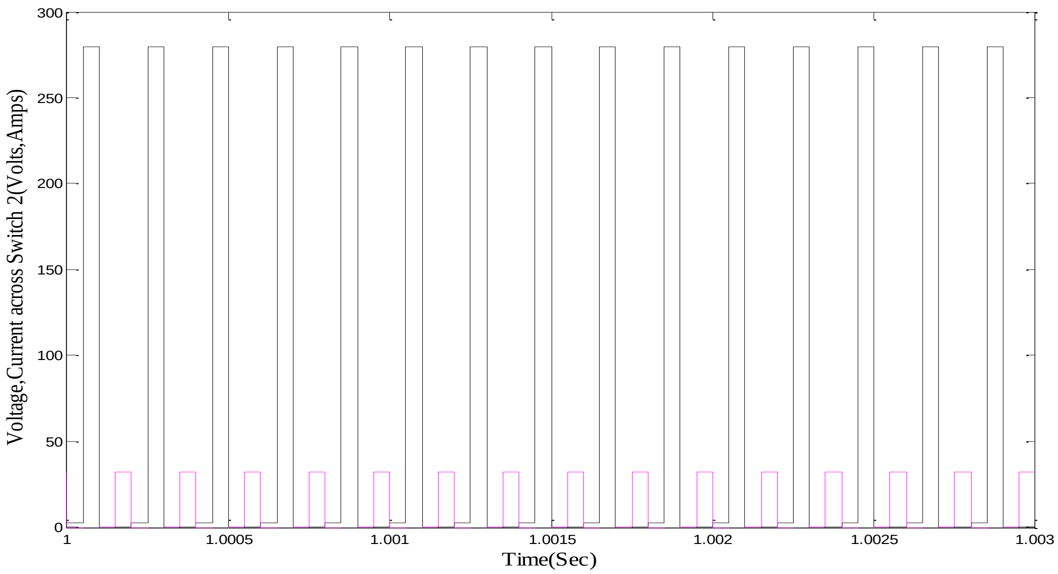
Graph 5.Voltage response of a ZVZCS Boost Converter across switch (S_U)

Graph 6 shows the DC current response of the ZVZCS based boost converter and the converter delivers an average DC current of switch S_U of 32 amps.



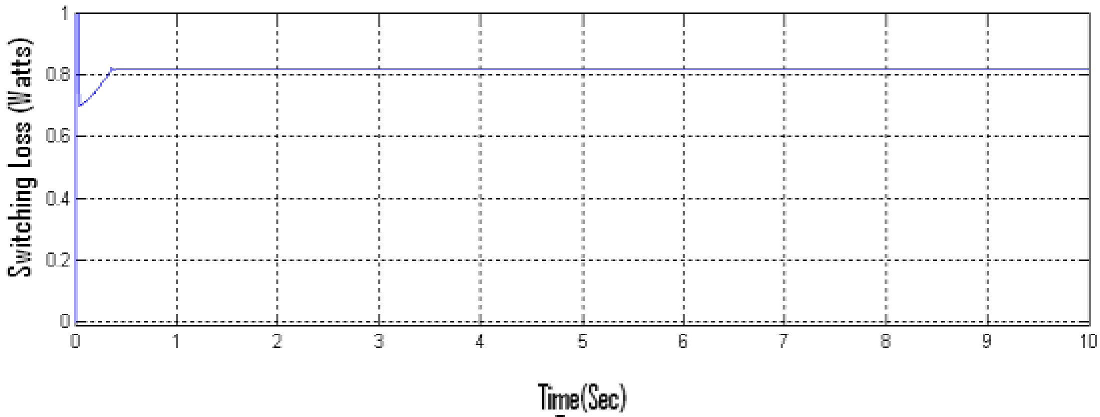
Graph 6.current response of a ZVZCS Boost Converter across switch (S_U)

Graph 7 shows the DC voltage, current response of the ZVZCS based boost converter and the converter delivers an average DC voltage, current of switch S_L of 280 Volts, 32 amps.



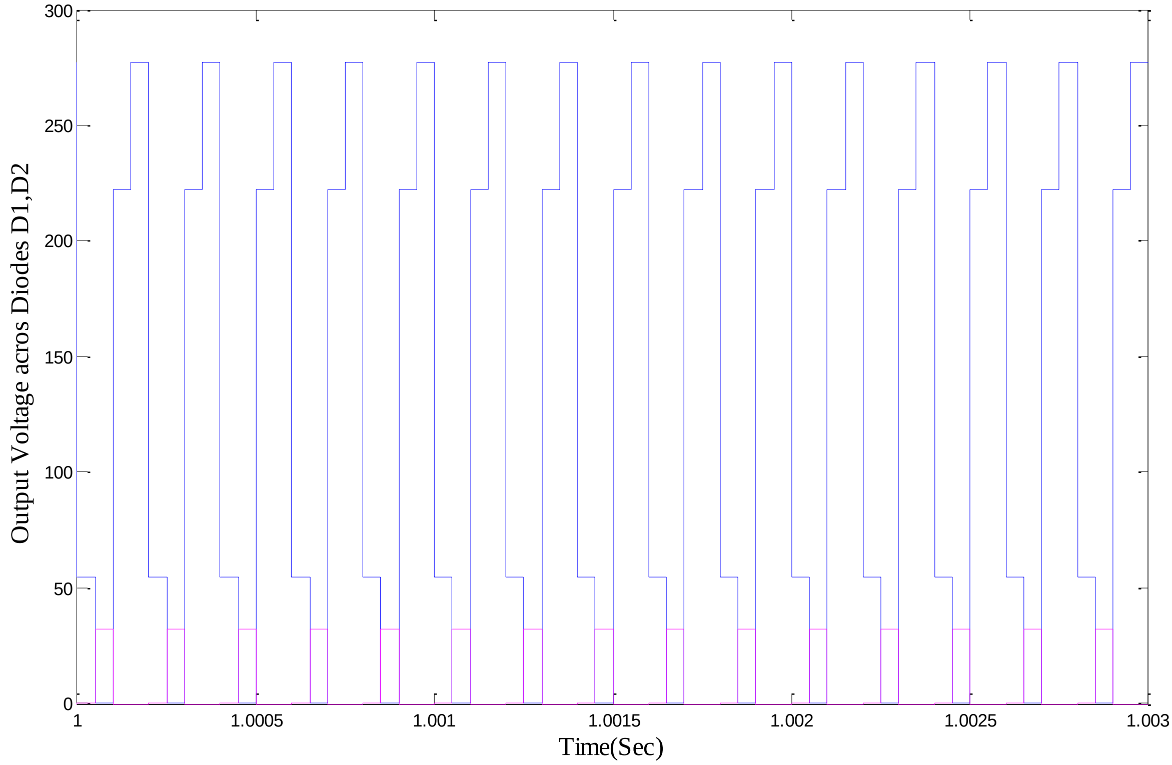
Graph 7.Voltage, current response of a ZVZCS Boost Converter across switch (S_L)

Graph 8 shows the average power loss across the MOSFET switch during the operation of the ZVZCS based boost converter and the converter dissipates an average power loss of 0.81 Watts across the switch. This power loss comprises of a small amount of the switching losses and major amount of conduction losses.



Graph 8 shows the average power loss across the MOSFET switch

Graph 9.Average Voltage, Current across the diode ($D_{1,}D_2$) of ZVZCS Based DC-DC boost converter



Graph 9.Average Voltage, Current across the diode ($D_{1,}D_2$) of ZVZCS Based DC-DC boost converter

Table1: Comparison of Performance of the Boost Converter and Proposed Design

Converter configuration	Boost Converter	Proposed Design
Input voltage(V)	70V	70V
Switching Frequency	15kHz	15kHz
Filter Inductance	1.5mH	$70\mu H$
Load Resistance	100Ω	70Ω
Output Capacitor	$500\mu F$	$10mF$
Output Voltage	360	560

CONCLUSION

A design is proposed in the paper for DC-DC converter for high step up and high power applications. From the simulation results it is observed. The voltage stress across the switches is much lesser. From the comparison of results with the conventional boost converter it is observed that the Capacitor size and inductor volumes are reduced in the proposed topology by adapting proper switching scheme. The switching frequency is also less which is an indication for reduced switching losses. The voltage conversion ratio is 1.5 times greater compared to the existing design and output power capability is also high. Therefore with optimum parameter selection and proper switching scheme, high power high step up voltage can be obtained in non-isolated DC-DC converter. Further the simulation results have to be validated through experimental results and optimization can be carried out using soft computing techniques.

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