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Simulation Analysis for Millimeter Wave Applications of Integrated Receiver System

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ABSTRACT

The objective of this research was to define a methodology for designing to presents the simulation analysis for millimeter wave application of integrated receiver system. A beauty thought of new design of CMOS LNA, filter and micro strip antenna are largely improves the system integration, reduced chip area and save the cost. In this paper, a three different architecture are proposed and analyzed through Agilent ADS tool. We have designed 90nm CMOS LNA at 40GHz to integrate with band pass filter and rectangular patch antenna at same frequency.

INTRODUCTION

Today, fastest growth of wireless communication industries is establishing a big new market opportunity. Current researchers are founding for new solutions which would be implemented into the existing wireless system networks to provide the broader bandwidth, the high quality and new added services. A millimeter wave (MMW) frequency band is the most promising technology for providing broadband wireless communications [1]. The extensive progress of CMOS technology has enabled its application in microwave and millimeter wave technologies. Presently, the CMOS technology has became one of the most attractive choices in implementing transceiver due to its low cost and high level of integration [2]. In spite of the advantages of CMOS technology, the design of CMOS transceiver in millimeter wave applications exhibits several challenges and difficulties that the designers must overcome. In addition, Kinetic performances of active devices with patch antenna have been improved, where MMW designs can be considered [7].
In RF receiver, the input signal from antenna first passes through the band pass filter to the LNA that amplifies it's and suppresses noise contributions from preceding stages. Hence, low noise figure and good impedance matching are essential.

LNA performance parameters while high gain are required by receiver system for achieve the system reliability. In present scenario, a 40GHz three stage of CG-CS LNA are designed using 90nm CMOS technology and integrated to Co-design of patch antenna with filter to achieve more than 20dB gain with good reverse isolation parameter that is enough to prove the system reliability. The basic geometry of complete receiver system are shown in Fig.1

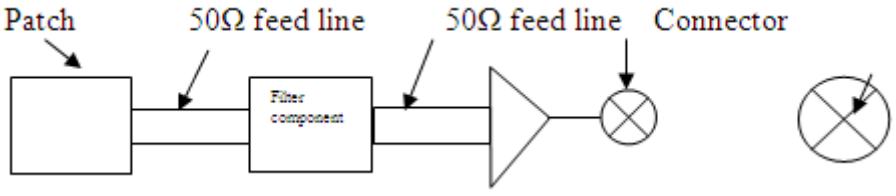

Fig.1 Basic geometry of LNA, filter and patch antenna

II. CMOS LNA ANALYSIS

As the fulfill requirements of LNA design, we can use the different topology like common source (CS), Common Gate (CG) etc. which are briefly discuss below.

CG-CS Topology

The common source (CS) and common gate (CG) LNA typologies are two popular architecture choices which are widely used for LNA design. The CS with the source inductor degeneration technique achieves the input impedance matching with the ideal noiseless components and gives to a minimal noise figure and also provides a higher gain whereas common gate has offers Wideband operating performance with good linearity and input-output isolation property [6]. But the parasitic capacitance of the transistor degrades the CGLNA performance in the higher frequency. The first stage of CGLNA is connected with the same next stage through a bonding wire can solve this problem and achieve the broadband operating performance which also holds the same beauties of the original CG LNA architecture at the same time [5]. Hence, we have design one stage CGLNA to achieve good reverse isolation with 50Ω proper impedance matching and single stage of CSLNA is added to the one stage CGLNA through a bonding wire which provides low noise and high gai

Circuit Design

A 40GHz two stage of CMOS LNA is designed using 90nm commercial TSMC design kit in Agilent advanced design system. Before proceed to LNA design, firstly we have analyzed the one stages of CGLNA with low Q factor and achieves the good reverse isolation (S_{11}) is -28dB and 50Ω input impedance with the help of equation given below and its simulation results are shown in Fig.3 and Fig.4 but sacrifice its noise figure and gain parameters.

$$Zin = \frac{1}{g_m + jwC_{gs}} \quad (1)$$

$$S_{11} = 20.\log_{10}\left(\left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right|\right) \quad (2)$$

For achieving the losses parameters (like noise figure, gain etc), we are using the next stage i.e. CS with source degeneration and achieved best gain of 26dB and minimum noise figure of 3.8dB which are shown in Fig.5 and Fig.6 as per specification of our design. Fig.2 shows the circuit schematic of the CMOS LNA at 40GHz. The cascode topology is used to reduce the miller effect, improve the stability and provides the higher power gain. The input-output match is accomplished with an LC impedance transformation network. The 208-fF output capacitor was implemented with two 218-fF capacitors in series to desensitize the process variation. Parasitic capacitances of input and output RF bond pads are also considered in the circuit simulation. In this simulation, we have chosen design specifications and technologies under low supply voltage of 1.8V are shown in Table1.

		Device Width(µm)	Length(µm)	Biasing(V)
M1		36	0.09	0.6
M2		21	0.09	0.72
M3		35	0.09	1.8

3 SIMULATION RESULTS

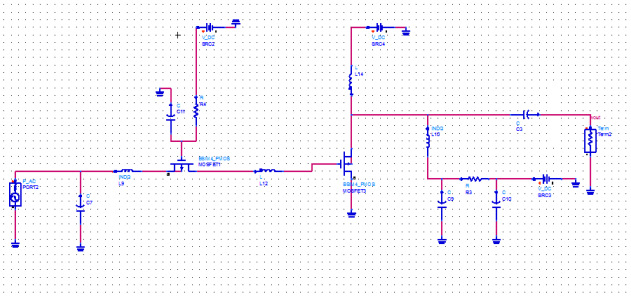

Fig.2 Schematic circuit of CG-CSLNA at 40GHz

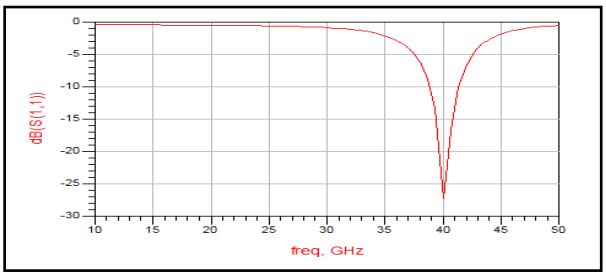

Fig.3 Return loss Vs frequency at 40GHz of LNA

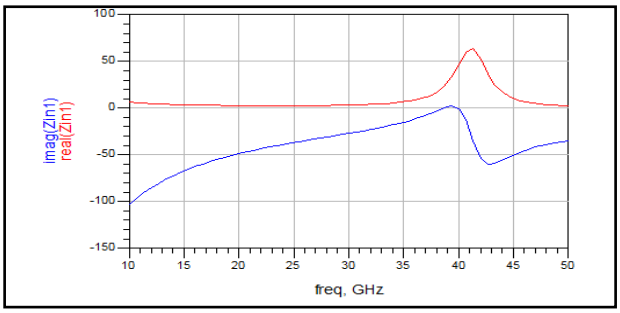

Fig.4 Input impedance variation with frequency of LNA

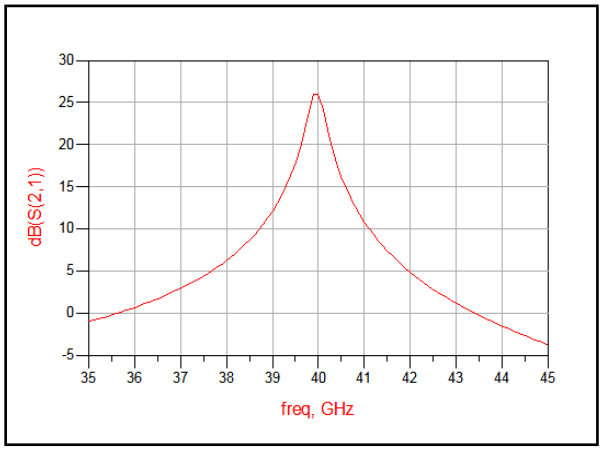

Fig.5 Forward gain Vs frequency of LNA

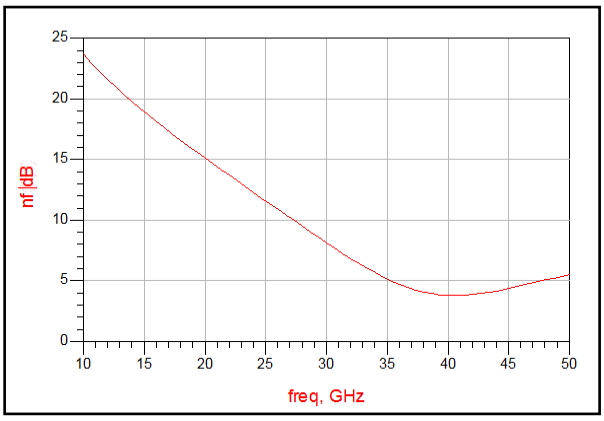

Fig.6 Noise figure Vs frequency of LNA at 40GHz

III. DESIGN CONSIDERATION OF THE ANTENNA AND FILTER

Rectangular Patch Antenna

The microstrip antenna is a small electrically antenna that has a number of advantages over the other antennas i.e. lightweight, inexpensive, and easy to integrate with active devices to improve the system reliability. In this paper, we have design a rectangular patch antenna at 40GHz with new type of feeding and simulated in ADS tool. All the design work taken a RT durroid substrate with thickness of t = 0.245 mm at the height h = 10mil above a lossless ground conducting layer. The dielectric between metal layers is assumed to have ϵ_r = 2.36 and tanδ = .002. At 40GHz, a 50Ω feedline given these parameters would have a width and length is 2mm and 0.7mm respectively and the final dimensions of the patch are a length L = 2.2mm and a width W = 2.4mm respectively. The resulting input impedance (Z_{in}) and return loss (S_{11}) are 50Ω and -13.08dB respectively. The 3D view of patch antenna with fabricated structure is shown in Fig.7

Butterworth BPF

The next stage precedes the LNA is butterworth band pass filter after the antenna which passes the desired frequency to the LNA in receiver system. The concept of filter is also used to achieve wideband operating performance of CGLNA

[3] [4]. The butterworth BPF are designed at centre frequency of 40GHz with attenuation pass band of 3dB to achieve S_{11} of 14dB which is below than -10dB and VSWR of 1.5 are given here in Fig.8 and Fig.9 respectively.

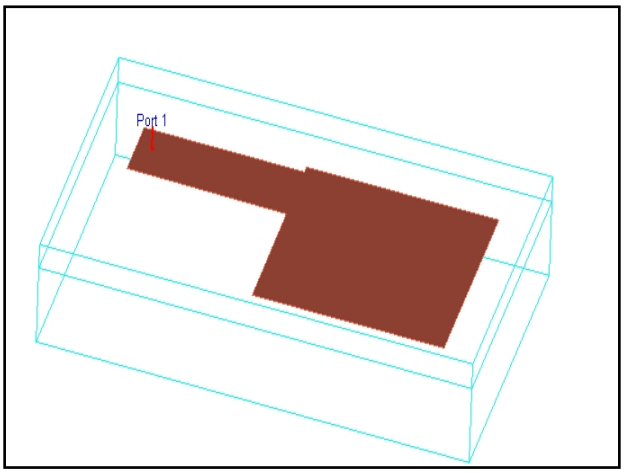

Fig.7 3D view of the designed patch antenna at 40GHz

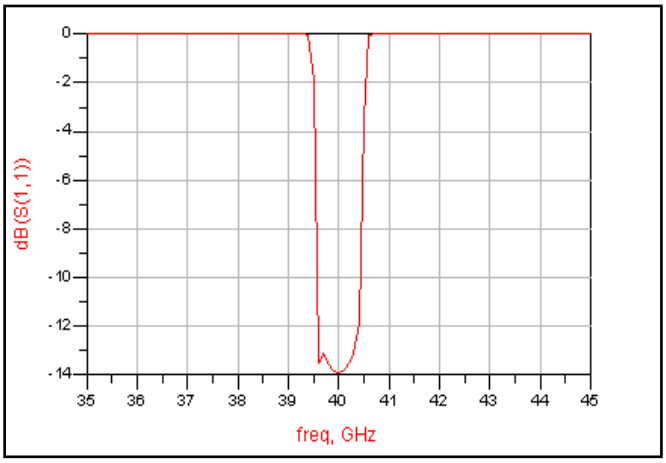

Fig.8 Return loss Vs frequency at 40GHz of filter

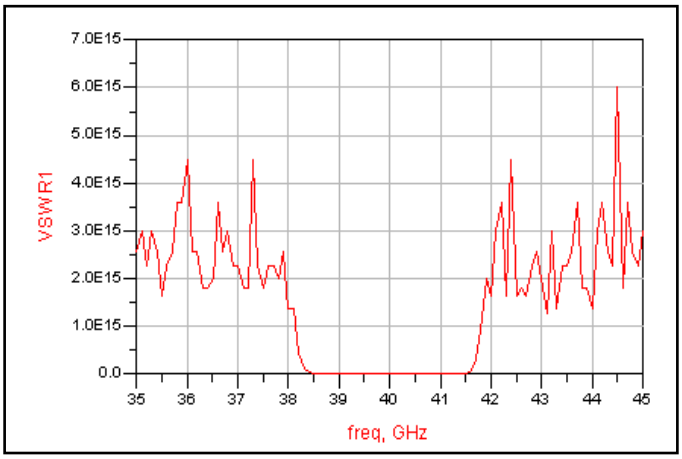

Fig.9 VSWR Vs frequency at 40GHz of BPF

CONCLUSION

The complete receiver system is designed for MMW applications in this paper, based on CMOS technology. The double-ended three stages of LNA are designed using 90nm CMOS process at 40GHz in this circuit. Performance standards are met for this new design technique. Simulation results of the designed circuit is shown that gain of 24dB, noise figure NF of 3.8dB, S_{11} of –33dB and VSWR of about 1.5 with the DC power dissipation of 25mW under 1.8V

power supply. The proposed method of receiver system in MMW applications, increases the level of system integration, reduces chip area and increases the overall system gain.

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