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Receiver for Transmission through TV Cable - A Comparative Study

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ABSTRACT: A very high speed LAN in the range of 500 Mbps throughput is proposed here for a cable length of 1 kilometer. It is compared against the nearest rival of 300 Mbps which is FDMA based. This paper addresses the design issues of the Direct Down Conversion receiver circuit in Q-Dot technology. We here make a comparison study between Frequency division multiple access and Code division multiple access to improve capacity which favors the mixer, filter and correlator design.

1.0 INTRODUCTION

The major challenge of today's data communication is to achieve higher bit rate than 100 Mbps. The cable bandwidth is 100 MHz, but using the full spectrum is difficult as CMOS cut off frequency is low. Thus CMOS circuit is not possible. Here we propose Q-Dot technology [1]. We need high speed and through put for internet and digital TV cable transmission. The technology is either frequency division multiplexing or code division multiplexing. In FDMA we propose a QAM transmission to double the capacity. In CDMA for a chip length of 7, we can easily achieve 4 times the normal capacity, with higher complexity of circuit design. In CDMA technology the performance is better for same occupied bandwidth as the data is integrated over a longer period. To circumvent this we propose differential signaling in FDMA.

Here we address the system design problem that will ease the filter design along with coherent demodulation. Also we try Q-Dot technology for switched capacitor circuit design. Switched capacitor circuit [2] has many applications in discrete time analog signal processing such as data converters. Similar problems can be solved by Q-Dot technology except it will work at much higher frequency. Moreover if the frequency remains same then it will occupy less area in layout design. If possible the Q-Dot will be a favored technology than CMOS/BJT. Here we propose two Direct Down Conversion methods for FDMA and CDMA with their circuits in Q-Dot technology. The section-I introduces the subject. In the section-II we check the capacity improvement and in the following section we choose the best design for capacity improvement. Section-IV discusses the various issues of Direct Down Conversion circuit. In Section-V we design the necessary circuits in Q-Dot technology. In the last section we conclude the paper.

2.0 CAPACITY IMPROVEMENT

In wireless communication, we transmit H (magnetic field) which attenuates inversely with distance. Now if we transmit Hx and Hy perpendicular to each other propagating in z direction, we get double the capacity. In LAN application it translates into transmission of a+jb, where $a \in (1, -1)$ and $b \in (1, -1)$. This means we have two components of current with a phase difference of 90 degrees. That means we have to distinguish the phase of the received signal. We can use QAM for double capacity.

In CDMA we can find that for PN code the autocorrelation is N for a time difference t = 0 and is -1 for a time difference t > [N/(N+1)]Tc. So we can have 8 such clusters with each cluster having 7 users. Hence the maximum cross correlation will be 6 which has to be kept in mind while designing the codes for the users. We design for three users and each transmitting 1 and -1 as two users. This will keep the cross correlation to minimum value. Thus we can have 4 times capacity in CDMA of code length of 7 which will not give cross-correlation. This is explained in Figure 1.

3.0 CHOICE OF TRANSMISSION

We know from previous section that we can get double the capacity by superimposing two signals delaying each other by 90 degree phase which means ½ Tb delay. On the other hand we can improve capacity 4 times or more by choosing CDMA

transmission. But we envisage a filter problem in the second scenario. We implement three filters. The first one is a band pass filter choosing 10 channels (for example). The second one is a RC filter we use in Sampling and Hold circuit. The third one is the Switched Capacitor filter. So we try to understand how a filter works. Assume the signal is x(t)=cos(wt)+cos(2wt)+cos(4wt). We want to attenuate frequencies more than w term by 20dB (for example) by a filter. So, the output of the filter will be y(t)=cos(wt)+0.1*cos(2wt)+0.1*cos(4wt). Here, the signal is cos(wt) and noise is 0.1*[cos(2wt)+cos(4wt)]. In reality signal will be integration of frequencies from 0 to w and noise is the signal attenuated out of band signal (integration of that). If we understand its implication we choose filter which rolls off.

The second filter is a RC filter which rolls of 20dB per decade frequency. Because of sampling it aliases back to the signal of choice. We made some rudimentary calculation and found the signal to noise margin is in the range of 6 to 12dB for equal power transmission in each other consecutive of the 10 channels. Thus for CDMA we have to attenuate 10*x to 1 even though RC filter is not a linear phase filter. It will be difficult to synchronize and the factor x is found by Monte Carlo simulation. We can use a normal analog filter but it requires OPAMP and precision resistance. The switched capacitor circuit uses OPAMP but with capacitors ratio which a controllable within 5% error. In Q-Dot circuit we do not use OPAMP but a voltage to Time conversion circuit (a comparator). The third filter is a switched capacitor filter and we follow G. Fischer's [3] method of implementing it either by Butterworth Filter or by Half Band filter. So we incorporate both the tricks and get higher capacity to be found out by simulation. We may use differential encoding to reduce the noise further. Now, for FDMA the third filter should provide an attenuation of 20 dB and for CDMA the attenuation required is 29 dB.

3.0 DIRECT DOWN CONVERSION CIRCUIT

The direct down conversion circuit is well known for FDMA transmission and is given in Figure 2. We choose consecutive 10 channels (for example) using a bandpass crystal filter. It is mixed with the center frequency wc (which varies for the choice of channel) and low pass filtered. This is fed to the voltage controlled oscillator to generate the wc frequency needed in the mixer. If there is no sample and hold circuit the filter will be analog and big. Moreover in digital communication we need a sampled signal to be detected. If we sample and hold it then there will be a RC filter whose group delay is nonlinear. This affects the FDMA circuit as well as CDMA circuit. In FDMA, the group delay distorts the signal of choice. But in CDMA, due to different delay for different frequency, the synchronism in cross-correlation in time domain is lost and higher cross-correlation may appear. Moreover the circuit for skewed clock has to be repeated for each channel as shown in Figure 3. If we increase the bit rate then generation of skewed clock will be a problem for CDMA. For CDMA we need additional circuit the correlator and an integrate-and-dump circuit followed by a comparator detector. These are for each user (56 for our case).

4.0 FILTER DESIGN

Designing the RC filter is simple as we get the value of C from KT/C noise and R from the corner frequency of 25 KHz [2][4]. It is sampled at 200 KHz with transition band from 25 KHz to 75 KHz. The design of switched capacitor filter could be Butterworth or Half-band filter implemented as direct IIR-form as mentioned in reference [3] shown in Figure 4 or as FIR filter[5]. We need delay cells and ratio adder circuit. For CMOS circuit, we need OPAMP which is not required in Q-Dot circuit. Figure 4 shows the modified IIR structure for implementing switched capacitor filter. It incorporates a delay between two analog adders. Thus the overall transfer function has an additional delay. If we transmit differential signal then the RC filter will have a very low value of R (corner frequency 1/2Tb) and we need to put another integrator. The Q-Dot can implement the delay cell as shown in Figure 5.

5.0 CIRCUIT ELEMENT

The circuit elements are analog delay circuit, adder, multiplier, mixer, VCO [6], correlator and integrator. The schematic of the circuits are given in Figure 5,6,7,8 and 9. We can implement a switched capacitor Q-Dot filter of second order Butterworth filter as shown in Figure 4. Mixer and VCO are given in reference [6] so the detail of those circuits is not given here. The delay locked loop required for generating skewed clocks are not given here. Figure 10 shows implementation of IIR filter by Switched Capacitor.

6.0 CONCLUSION

A comparative study of implementation of high speed data transmission is given here. The simple FDMA technique has a capacity 300 Mbps in a 100 MHz bandwidth using a 4QAM modulation. The complicated CDMA circuit can get higher

capacity nearly 500 Mbps. We need to run it at half the rate for proper detection which will be decided by the accuracy of the filter and correlator. The choice of design will be decided by the compactness of the layout design for all parallel paths.

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FIGURES USED

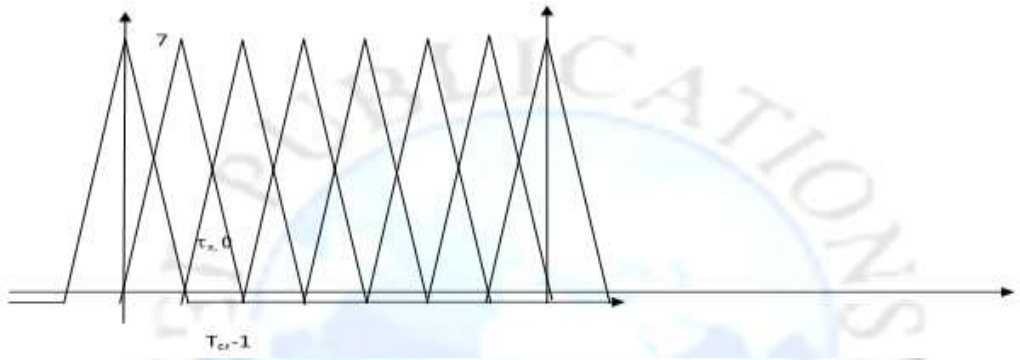

Figure 1. Correlation of different users signal with different delays

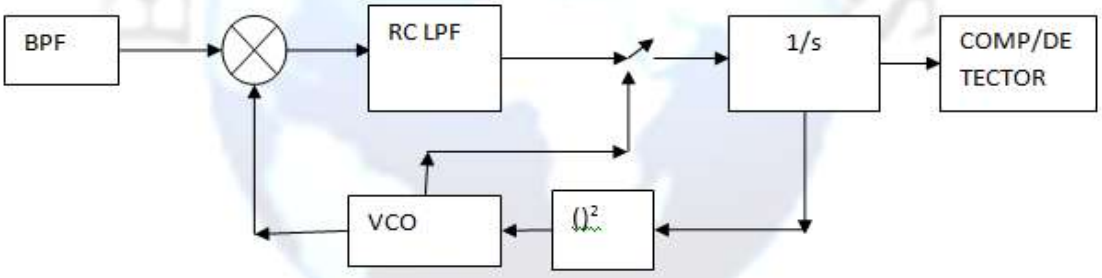

Figure 2. Direct down conversion of FDMA signal

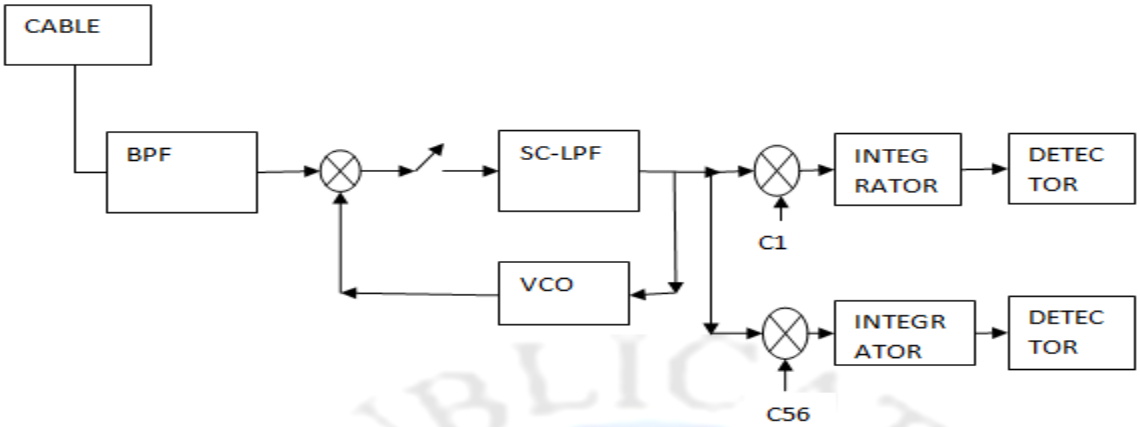

Figure 3. Direct down conversion of CDMA signal

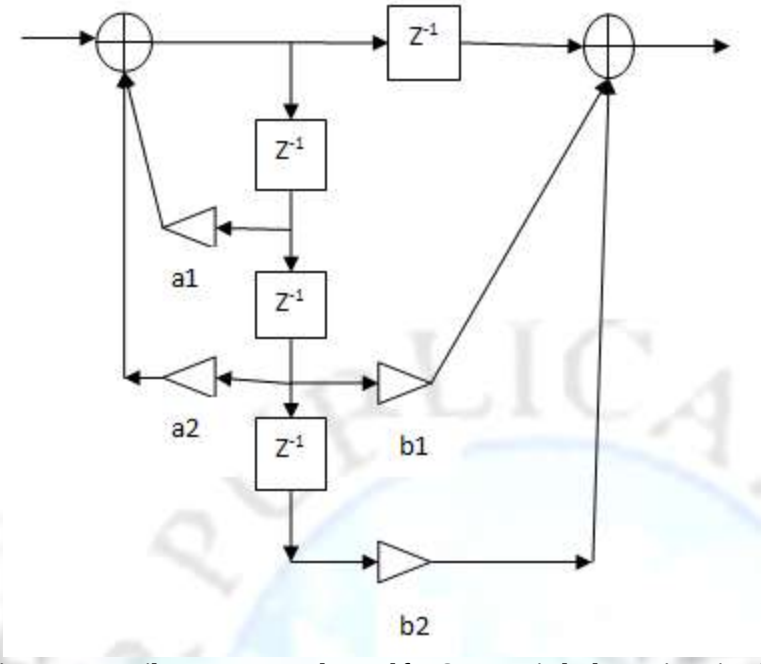

Figure 4. IIR Filter structure to be used for Q-Dot switched capacitor circuit.

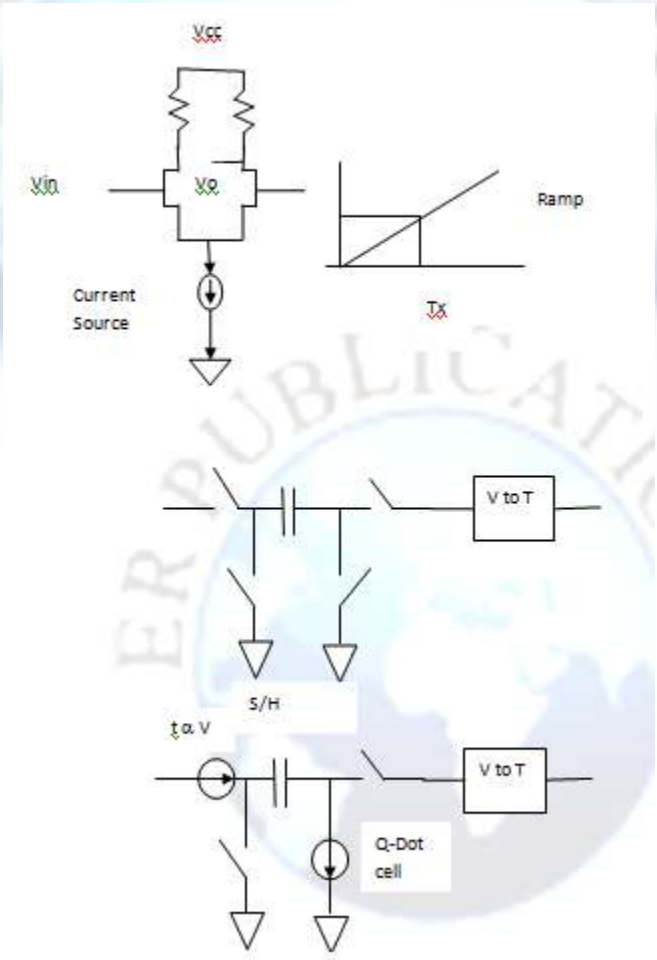

Figure 5. Delay cell implemented in Q-Dot circuit.

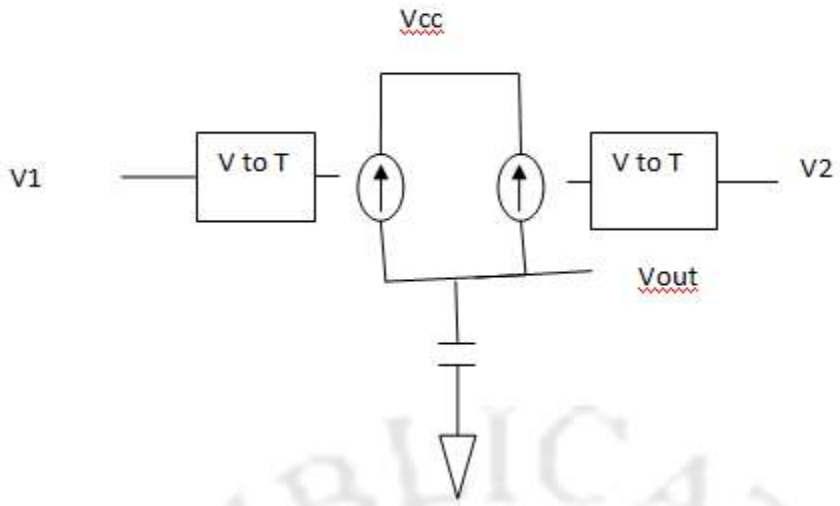

Figure 6. Adder Circuit

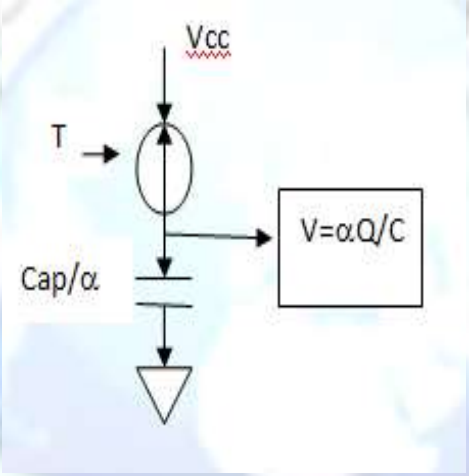

Figure 7. Implementation of multiplier by scaling the capacitor.

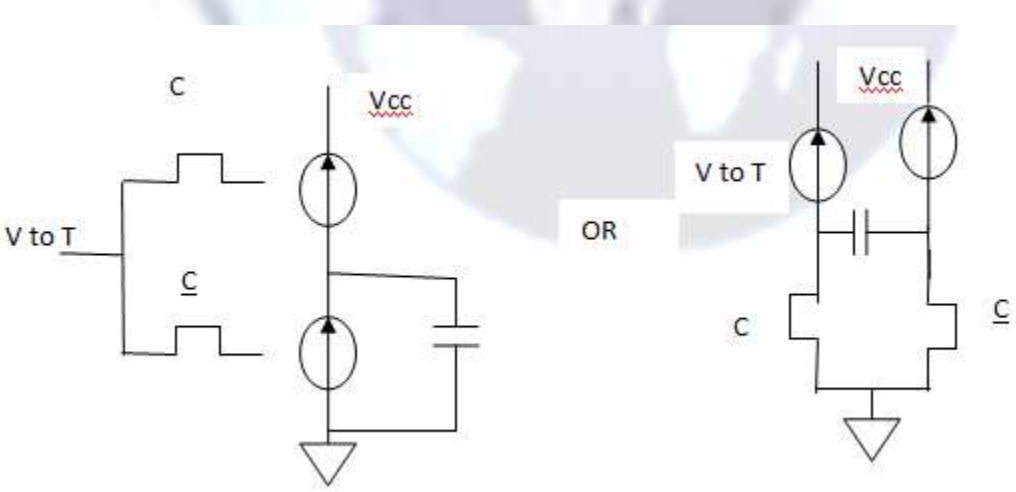

Figure 8. The correlator circuits.

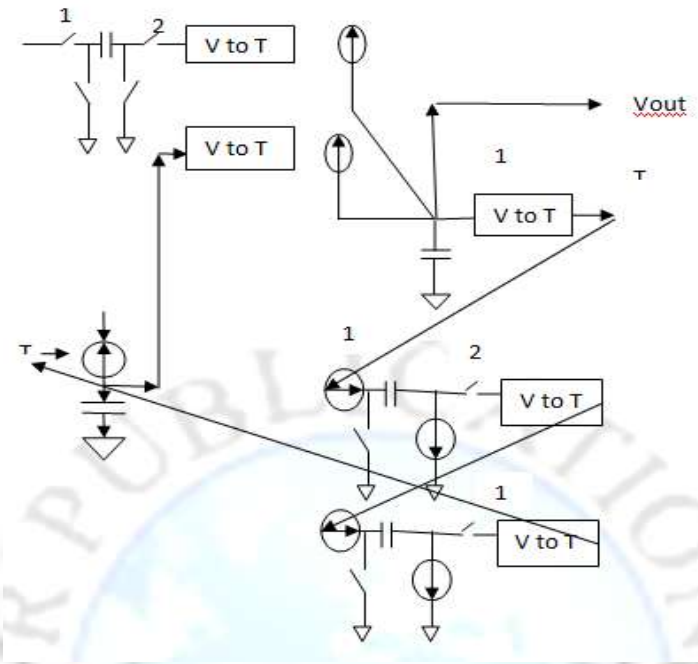

Figure 9. The integrator circuit.

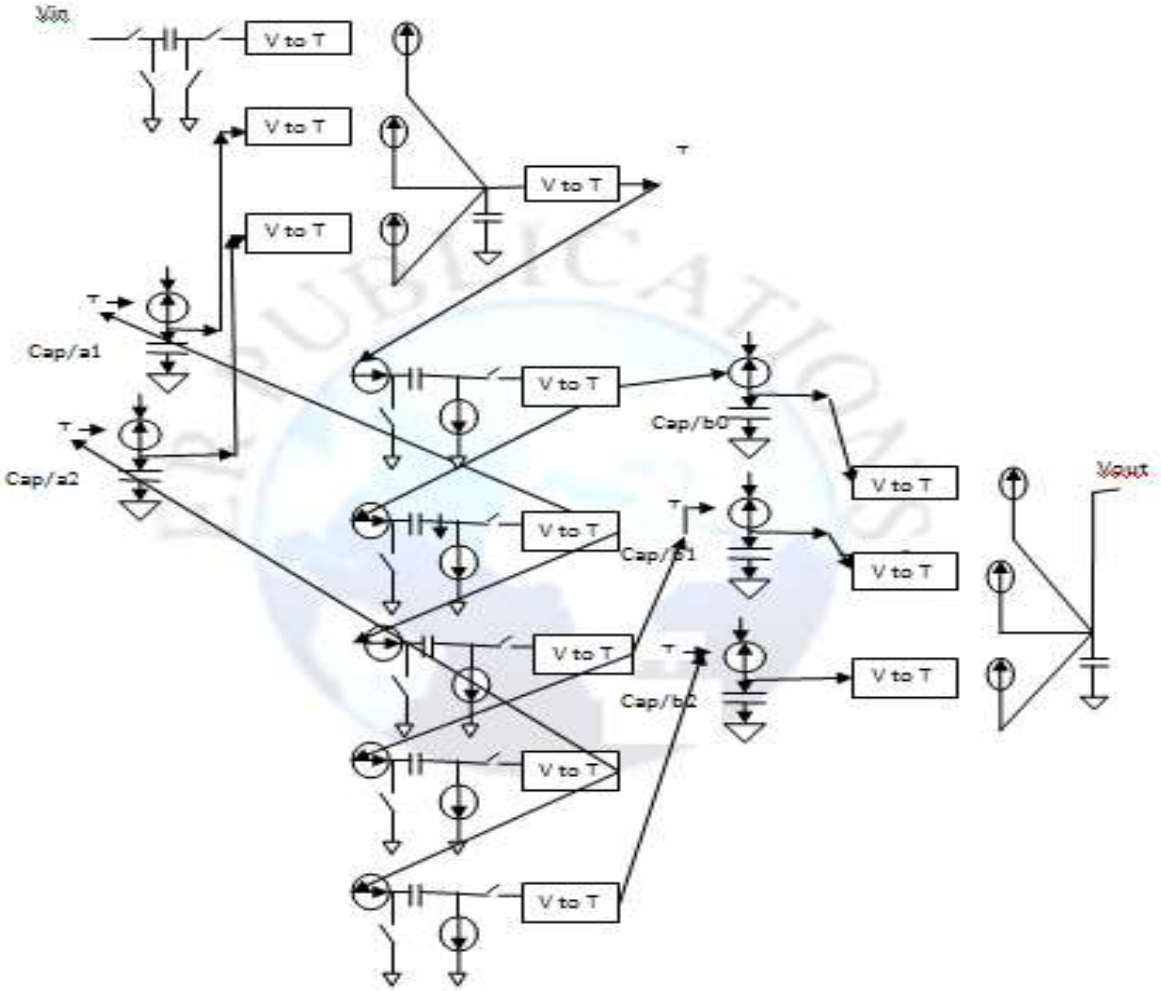

Figure 10. Second order IIR filter in Q-Dot circuit.