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# A study on design and analysis of SRAM & DRAM

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**Abstract: In this paper, design and analysis of 8Mb SRAM is described focusing on optimization of power and delay. The used technology is 90nm. The access path of SRAM is divided into two parts: first is from address input to the word line rise (the row decoder) and second is from word line rise to data output.**
**The key parameter for low power operation in SRAM data path is to reduce the signal swings on the high capacitance nodes i.e. bit lines and word line. Circuit partitioning, gate oxide thickness variations and low power layout techniques are used to minimize the power dissipation while designing SRAM. In this paper, 8Mb SRAM is built up of two memory cuts, each of 4Mb along with the control logic and the decoding sections. The main aim of this project is to minimize the power consumption. To reduce the power dissipation in active mode decoder is implemented as a tree structure while a multi Vth technique is used to reduce power in standby mode.**

**Keywords: SRAM, DRAM, cells, 16-bit operation, analysis.**

## 1. Introduction

A basic SRAM cell consists of two cross coupled inverters which act as a simple latch as storage elements and two switches connecting these two inverters to complementary bit lines to communicate with the outside of the cell (figure2.1)

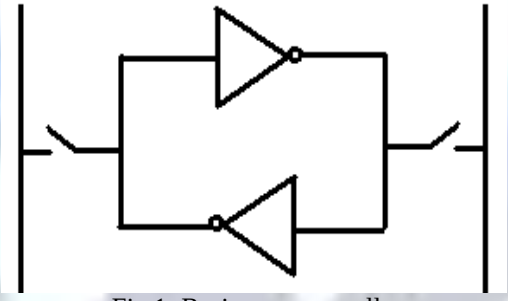

Fig.1: Basic memory cells

Two switches in figure 2.1 are NMOS pass-transistors, which are controlled by a word line. As long as the pass-transistors are turned off, the cell keeps one of its two possible steady states. The structure shown in figure 2.1 is symmetric and both bit lines BL and BL take part in read and write operations. Common word line (i.e., WL) controls accessibility to the cell nodes Q and QB through two-pass transistor during reading or writing [1].

To perform the write operation into an SRAM cell, the value and its complements are loaded onto the bit lines by write circuit and the word line is raised simultaneously. To read a value from an SRAM cell, both bit lines are precharged high and the word line is raised turning on the pass transistors. The bit line relative to the cell node that contains 0 begins discharging. The sense amplifier, which is connected to the bit lines, detects which of the bit lines is discharging and hence reads the stored value. The 6T-SRAM Cell is shown below in fig. 2.

**Read Operation:**

Assume that we want to read '1' means a 1 is stored at Q node and a 0 is stored at QB. Also, assume that both bit lines are precharged to Vdd before the read operation to be performed. The read operation should be started by asserting the word line, which enables the two pass-transistors M 5 and M 6 (see figure 2). Consequently, the contents stored at Q and QB begins to transfer to the bit lines BL and BLB respectively. BL remains at its precharge value while BLB will be pulled down to the

ground by discharging through M5 -M1. A careful attention should be paid in sizing of transistors to prevent unexpected writing a zero into the cell [2].

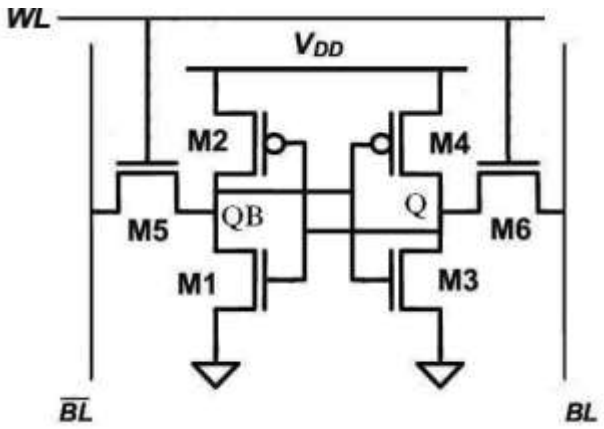


Fig: 2 6T- SRAM Cell [3]

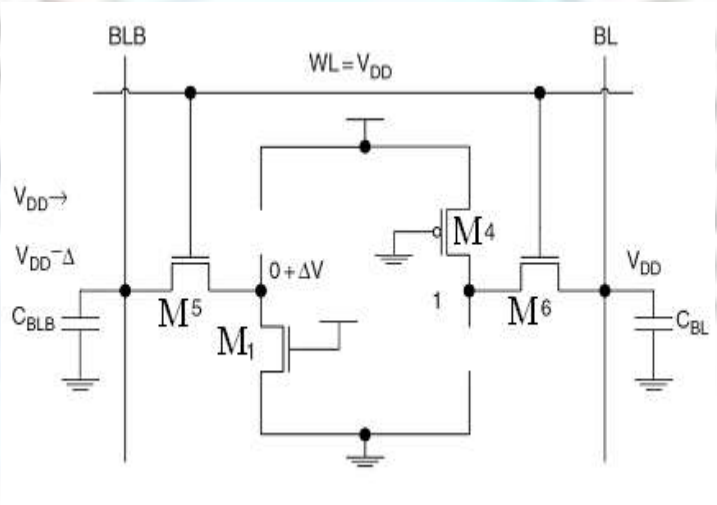


Fig:3 Read Operation of 6T- SRAM Cell [3]

Consider the BL side of the cell. The capacitance of the bit line for larger memories is significant. Upon enabling the WL, initially BL stays in its precharged value Vdd. The path composed of M5-M1 pulls down the bit line towards ground. As we would like to have a minimum size cell, these transistors should be chosen as close to minimum as possible, which cause slow discharge of bit line capacitance immediately when a small difference is created.

At the beginning, when the word line is rising, the intermediate, QB, is pulled up toward the precharge value of bit line, BLB. This voltage rise must be kept as low as possible with careful sizing of transistors not to cause sufficient current derive through M3 -M 4 inverter, which may cause flip in the cell state. To avoid this from happening, the resistance of pull-down transistor, M1, must be less than that of pass transistor M5. This can be quantitatively obtained by solving the current equation at the maximum allowed value of voltage rise at node QB, which is the transistor threshold (of about 0.3 V). In other words, having less resistance for M1, it must be stronger than access pass transistor. This means that the following relation must be satisfied [3].

$$\beta = CR = \frac{W_1/L_1}{W_5/L_5}$$

**Write Operation:**

The write operation is similar to a reset operation of an SR latch. A write driver drives one of the bit lines, BL in Figure 4, from precharged value ($V_{dd}$) to the ground through transistor $M_6$. If transistors $M_4$ and $M_6$ are properly sized, then the cell is flipped and its data is effectively overwritten. A statistical measure of SRAM cell write ability is defined as write margin.

Write margin is defined as the minimum bit line voltage required to flip the state of an SRAM cell .The write margin value and variation is a function of the cell design, SRAM array size and process variation. A cell is considered not write able if the worst-case write margin becomes lower than the ground potential. Note that the write operation is applied to the node storing a "1". This is necessitated by the non-destroy read constraint which ensures that a "0" node does not exceed the switching threshold of inverter $M_2$−$M_4$.

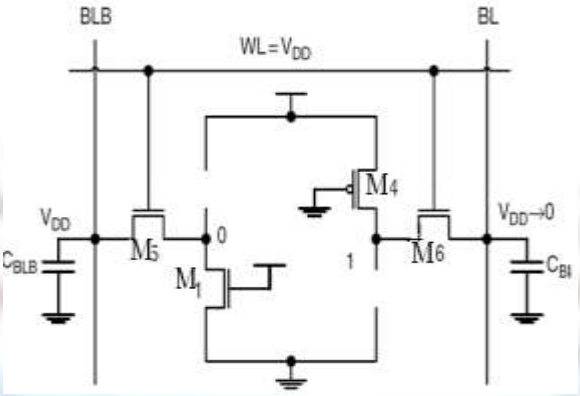


Fig: 4 Write Operation of 6T- SRAM Cell

The function of the pull-up transistors is only to maintain the high level on the "1" storage node and prevent its discharge by the off-state leakage current of the driver transistor during data retention and to provide the low-to-high transition during overwriting [4].

## LITERATURE SURVEY

Vinay Saripalli performed a work, "Variation-Tolerant Ultra Low-Power Heterojunction Tunnel FET SRAM Design". Author provides an analysis of 8T and 10T TFET SRAM cells, including Schmitt-Trigger (ST) based cells, to address these shortcomings. By benchmarking a variety of TFET-based SRAM cells, Author show the utility of the Schmitt-Trigger feedback mechanism in improving the read/write noise margins, thus enabling ultra low-VCC operation for TFET SRAMs [5].

Evelyn Grossar performed a work, "Statistically Aware SRAM Memory Array Design". In this paper, Author propose a method to minimize the leakage power of a SRAM cell while satisfying conflicting functionality and delay constraints, under these technology variations. Additionally, this method generates power-stability tradeoffs to optimize the circuit for a given yield at design time [6].

Matthias Jung proposed "TLM Modeling of 3D Stacked Wide I/O DRAM Subsystems". In this paper, Author present a new methodology using virtual platforms to model the backend of a 3D-DRAM memory subsystem (channel controller and Wide I/O DRAM) with special System C TLM2.0 phase extensions. This methodology enables us to explore the complete design space of memory controllers at the system level at very fast simulation speeds with precise timing accuracy [7].

Zheng Guo presented "FinFET-Based SRAM Design". Intrinsic variations and challenging leakage control in today's bulk-Si MOSFETs limit the scaling of SRAM. Design tradeoffs in six-transistor (6-T) and four-transistor (4-T) SRAM cells are presented in this work. It is found that 6-T and 4-T FinFET-based SRAM cells designed with built-in feedback achieve significant improvements in the cell static noise margin (SNM) without a re-penalty [8].

Yirong Zhao evaluates the static noise margin, leakage current, & read/write performance of these structures with the predictive technology model for FinFETs. Presented results show that single-ended multi-port FinFET SRAMs with isolated read ports offer improved read stability and flexibility over the double-ended structure at the expense of write performance [9].

## PROPOSED SYSTEM

The schematic of 6T-SRAM Cell is shown below in fig:5. When the input voltage Vin becomes high (logic '1'), the output of the first inverter becomes low (logic '0'). Since the output of first inverter is, applied to the second inverter, therefore it become on and the output of second inverter goes to logic '1'.When the word line signal 'wl' is asserted both the pass-transistor becomes turn on and the output of the both inverter passes through the pass transistor and appear at the bit lines blb and bl [10].

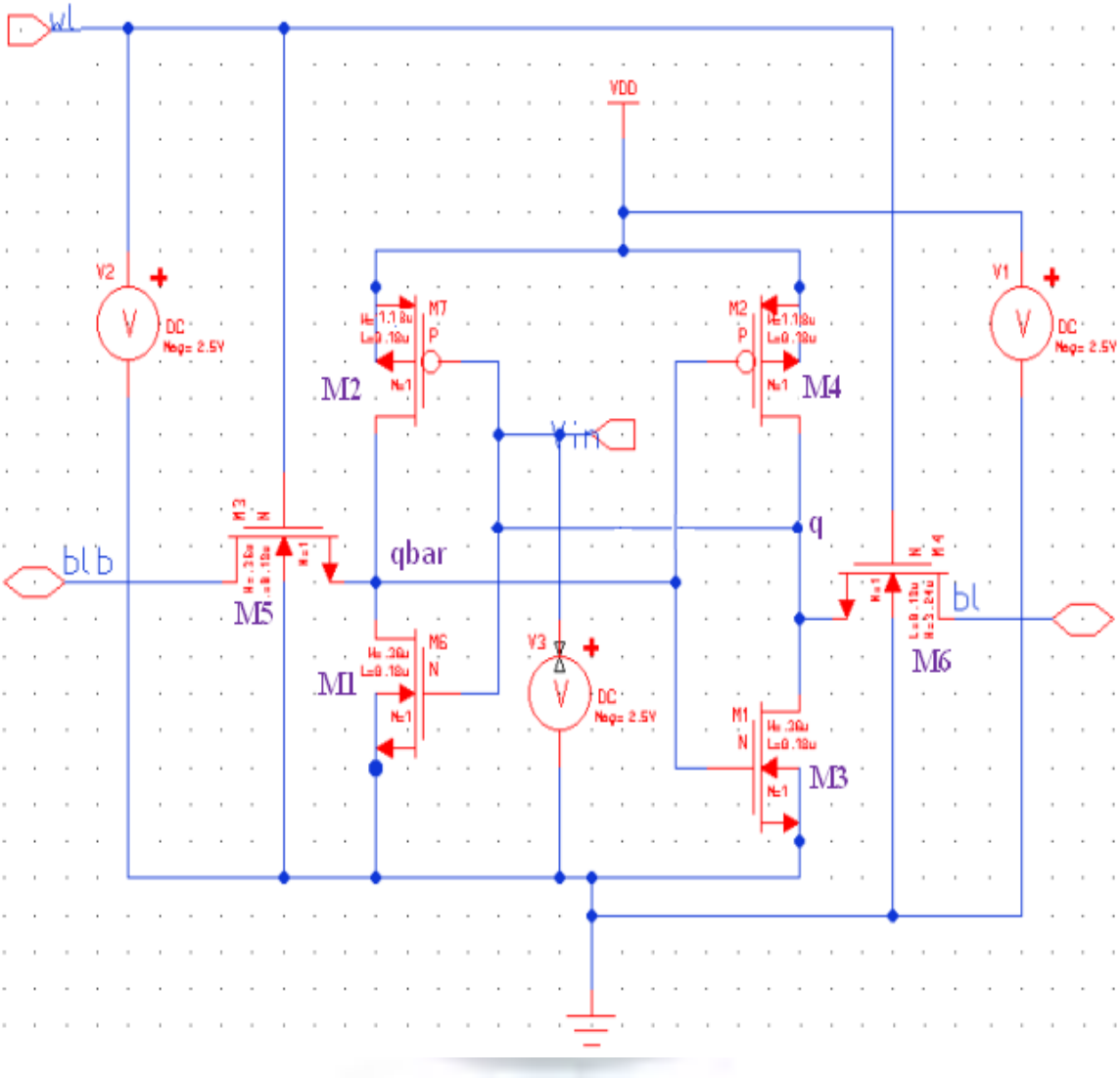


Fig: 5 Schematic of 6T- SRAM Cell

### SRAM with Precharge Circuit

The function of precharge circuit is to pull up the voltages on the bit lines respected to their voltage levels. Initially precharge circuit is off. When the input signal Vsel and word line signal 'wl' is high the NMOS transistor becomes on and complementary values that are given through bit lines are passes through the pass transistor and stored at the nodes 'q' and 'qbar' i.e. '0' on blb side and '1'on bl side. This is the write operation in the SRAM Cell.

To perform read operation firstly 'pcb' signal becomes low, which turn on the pre-charge circuit. Now the voltages on the bit lines blb and bl. become equalized. Read operation starts by disabling the pre-charge circuit and enabling the word line 'wl'. This causes the bit line BLB to decrease at a linear rate while the other bit line BL remains at high value i.e. constant that is shown in the waveform [11]. The schematic of the SRAM Cell with pre-charge circuit is shown the fig 6.

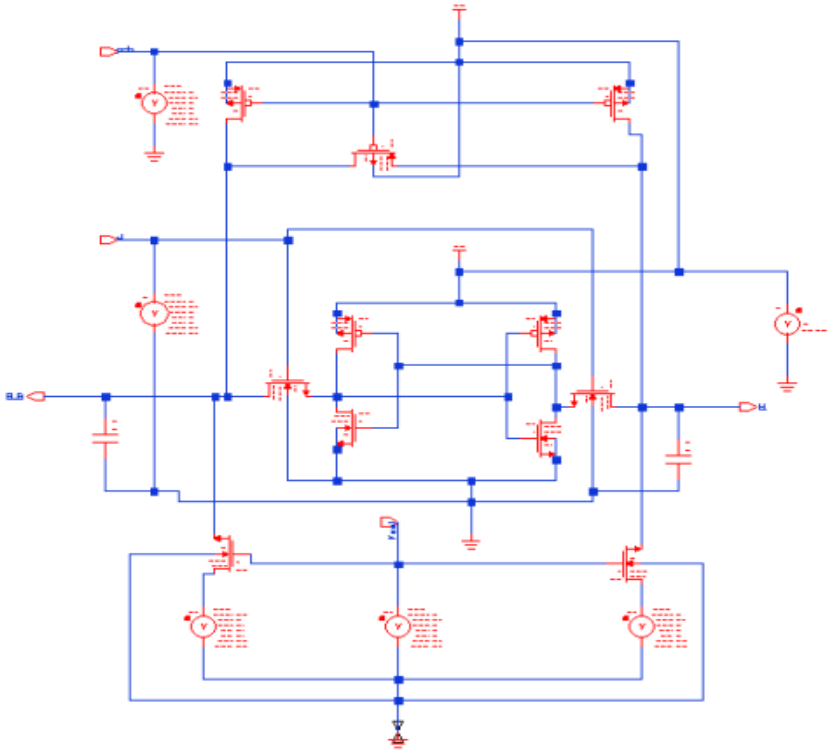

Fig: 6 SRAM Cell with Pre-charge circuit

**16-bit SRAM Memory:**

To implement 16 bit SRAM memory a 2-4 row decoder and 2-4 column decoder is used. It is arranged in 4x4 matrix form. Here the outputs of the row decoder are connected to the SRAM cells word line 'wl' and the bit lines of all cells are connected to the column decoder. When the input to the decoder is 00, the word line 'wl' of first row become high and all the SRAM cell are connected to the bit line [12].

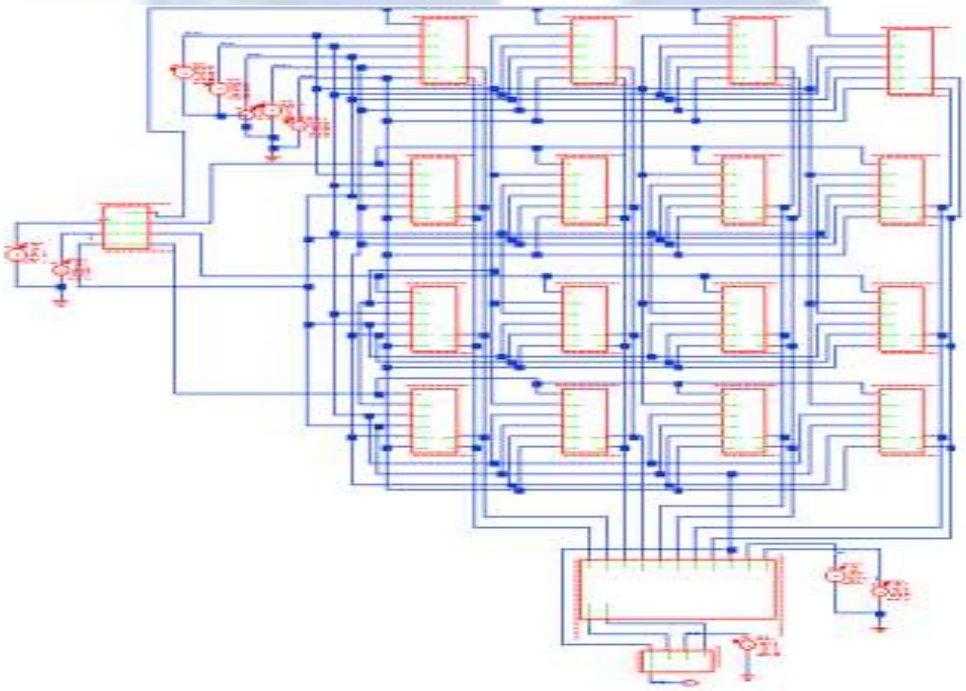

Fig. 7: 16-bit SRAM Cell

But depending upon the address of the column decoder one column will be selected. In this way a particular cell of the SRAM memory array will be selected. For example if '00'will be the address for both row decoder and column decoder, then a particular cell whose location is '00' in the memory array will be selected. If address of the row decoder is '00' but the address of the column decoder is '01' then second SRAM cell of the first row is selected. Similarly if the address of row decoder is '01' and column decoder address is '00' then $V_{out1}$ of the 2-4 decoder will high and first SRAM cell of the second row is selected. Power dissipation of this circuit is 3.0506 M watts [13].

The schematic of 6T-DRAM Cell is shown below, When the input voltage Vin becomes high (logic '1'), the output of the first inverter becomes low (logic '0'). Since the output of first inverter is, applied to the second inverter, therefore it become on and the output of second inverter goes to logic '1'.When the word line signal 'wl' is asserted both the pass-transistor becomes turn on and the output of the both inverter passes through the pass transistor and appear at the bit lines blb and bl.

**Waveform of DRAM cell**

The waveform of DRAM Cell for both dc analysis and transient analysis is shown below in the fig: 8 and fig: 9 respectively.

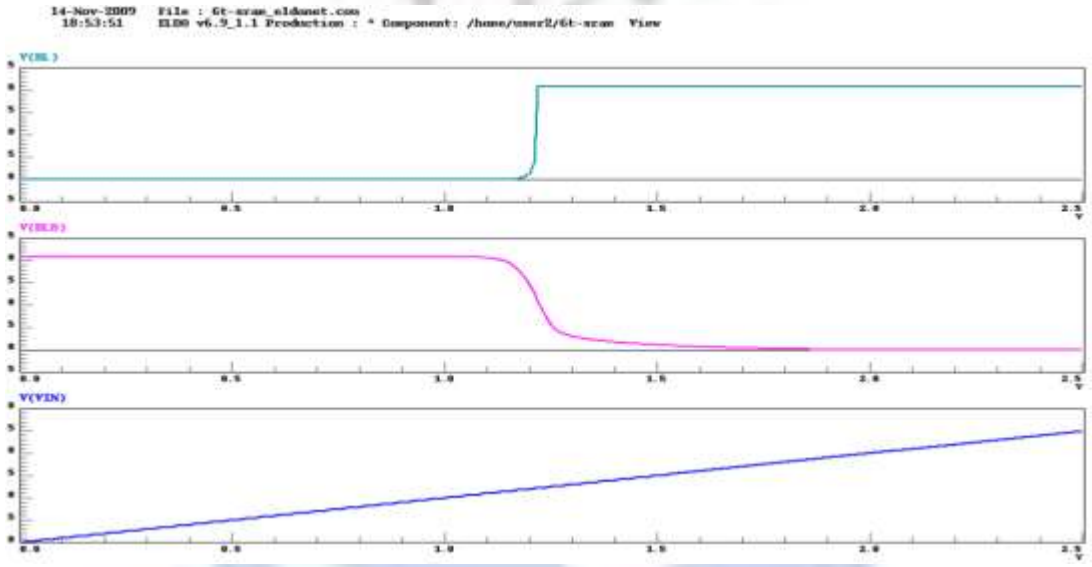


Fig: 8 DC Waveform of 6T-DRAM cell

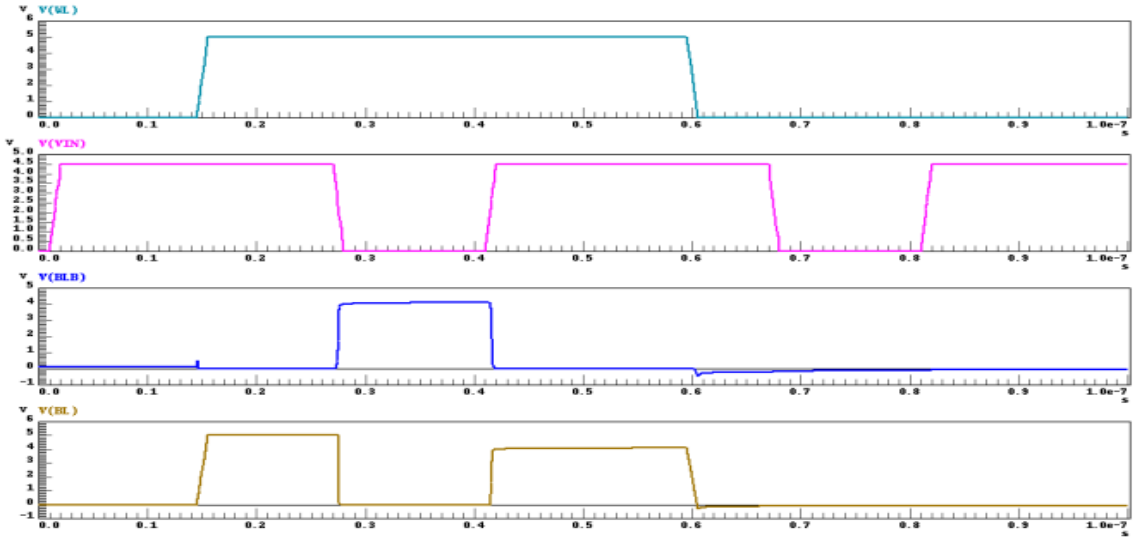


Fig: 9 Transient Waveform of 6T-DRAM Cell

From the waveform it is clear that both bl and blbar are complementary of each other [14]. When bl is at logic '0', blbar is at logic '1'.

## Conclusion

In this manuscript, the author have discussed a SRAM cell, differential voltage sense amplifier, precharge circuit, 2:4 block decoder ,3-8 row decoder 5-32 column decoder, 1Kb memory circuits both containing memory bank and without memory bank and simulate all these circuit using eldonet in 180 nm technology. For SRAM cell we have calculate SNM, DRV RM and WM. We have also done power and temperature analysis for different value of Vdd. In sense amplifier CMRR, delay and power are calculated for different value of Vdd and sensitivity is calculated at different value of threshold voltages. Delay and power are also calculated for decoder. We have done comparison between memory circuits both containing memory bank and without memory bank and find that the architecture containing memory bank has less power dissipation in comparison to the memory architecture without memory bank.

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