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Design of low power, high speed full adder using PTL-TG Hybrid style

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Abstract: **Full adders are essentially used as a building block in all arithmetic, DSP and microprocessor applications. In this paper, a 15 transistor hybrid PTL-TG full adder circuit is proposed. The main objective is to provide high speed, low power, full swing operation with good drivability. The choice of logic design affects the circuit performance. The delay time depends on the number of transistors used and design complexity. The power consumption depends on size of transistors. The proposed adder consists of a hybrid circuit using pass transistors, CMOS gates and transmission gates. The design is simulated using TANNER EDA v14 simulation tool. The performance is measured in terms of power, delay and Power Delay Product (PDP). The analysis has been done using 180 nm CMOS technology. Performance has been compared for variation of Supply voltage [1.2V-1.8V] at 200MHz frequency with 1fF load conditions. The reduction in power and delay is necessary for applications of full adder in low power, portable devices. The proposed hybrid adder shows better performance as compared to existing DPL and SR-CPL adders and it shows significantly low Power, delay and PDP. The proposed hybrid adder shows fully restored output logic levels. Utilization of a hybrid technique allows us to achieve the individual advantages of pass transistors and transmission gates and avoid the limitations of both designs. A 2 bit ripple carry adder is designed using proposed adder.**

Keywords: **PTL-TG, Full Adder, Power, Delay, PDP, Hybrid full adder, Tanner EDA.**

I. INTRODUCTION

The one-bit full adder circuit is one of the most widely used building blocks in all data processing (arithmetic) and digital signal processing architectures [2] and microprocessors and data processing subsystems. Adders form important components in systems performing arithmetic systems such as compressors, parity checkers, comparators, ALU etc. System performance of such a complex system can be enhanced by enhancing the performance of Full Adders. Nowadays power and delay are primary concerns for low power battery operations and portable devices. Optimum designing of full adder affects overall device performance of these devices. Full Adder takes three inputs A, B, Cin and gives two outputs Sum and Carry.

Mathematically,

So= A XOR B XOR Cin

Co= AB + ACin + BCin

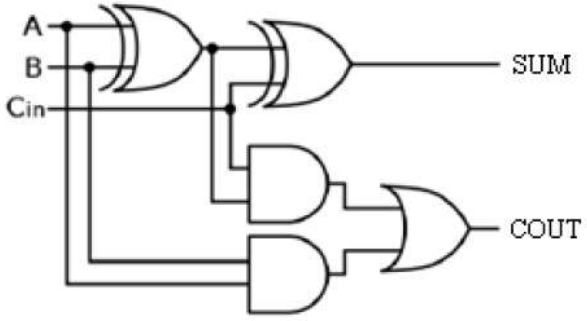

Figure 1: Block Diagram of Full Adder

Table 1: Truth-Table for Full adder

Cin	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The paper is organized as follows. In section II, we discuss existing DPL and SR-CPL hybrid adders. In Section III , Our Proposed hybrid adder is discussed. Section IV, a 2 bit ripple carry adder using our proposed hybrid adder is designed, Section V explains the design and implementation results. In section VI conclusion is discussed.

II. EXISTING HYBRID ADDERS

As various full adder designs have their own advantages and disadvantages, hybrid adders are made using two or more elementary designs to achieve low power dissipation, propagation delay and other enhancements.

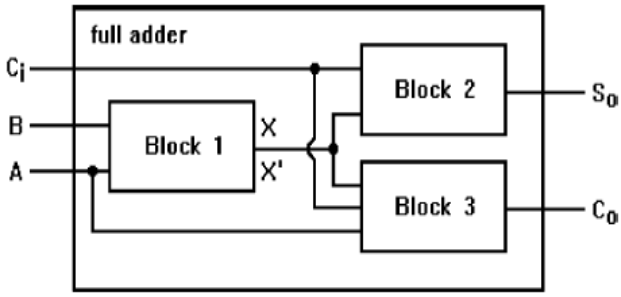

Figure 2. Full Adder formed by three main logical blocks [6]

Full Adder consists of three main blocks in its operations, one for the XOR/XNOR operation. i.e. block 1 . Block 2 is used to generate sum out by using the intermediate XOR/XNOR signals. Block3 is used to generate the Carry out. Pure designs use one logic for its operation. HYBRID Adders uses more than one topology for adder operation to achieve advantages of each topology. Hybrid adders take two or more best available schemes and combine them in an efficient way to achieve lower average power dissipation, delay and PDP. The main aim is to reduce the number of transistor count and power dissipating nodes and redundant elements.

Various example of hybrid adders are considered in [5] [8]. They are designed using Low power XOR/ XNOR gates and pass transistors or transmission gates logic for creation of sum and carry. Pass transistors reduces the number of transistors and TG LP design are very low power consuming and faster. Here A, B, Ci are the inputs and So and Co are the outputs. It should be noted that when A=B the carry output is equal to their value. If $A \neq B$, we have Co = Ci (the full adder is said to be in propagate mode), and, hence, the full adder has to wait for the computation of Co [6].

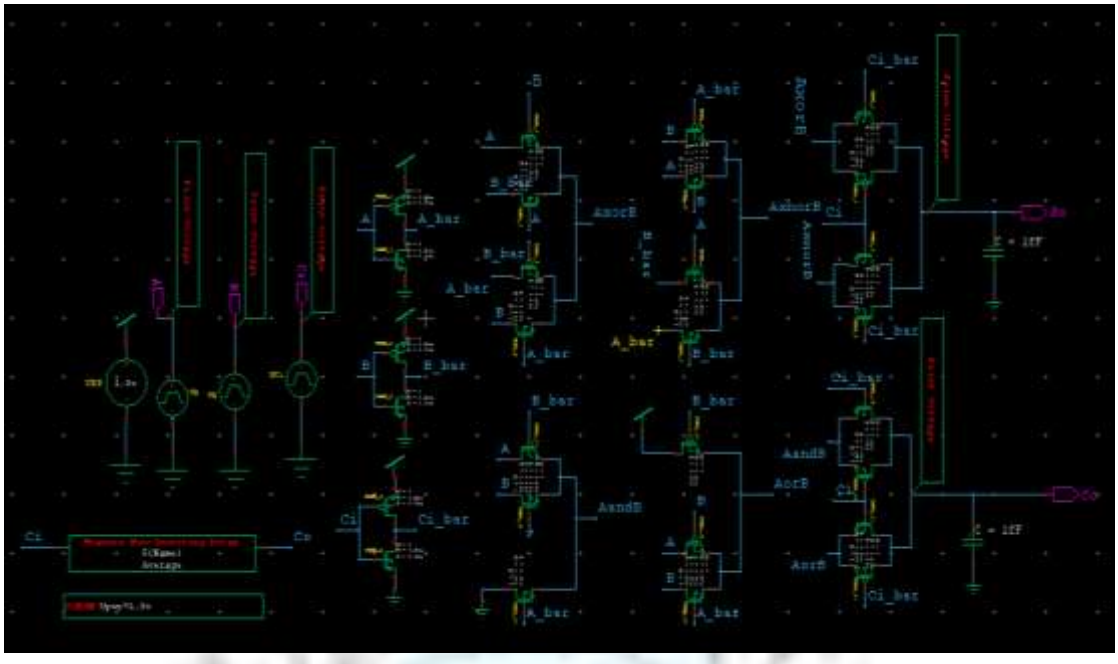

Figure 3. Schematic diagram of DPL-FA full adder[7]

DPL logic style uses the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output. The short-circuit consumption optimization is related to the powerless/groundless configuration of the constituent AND/OR gates, and the dynamic consumption optimization comes from the fact of reduced capacitances in the internal nodes for pass-transistor logic styles, and for the well balanced propagation delays inside the full-adder, which results in less glitches at the outputs.[7]

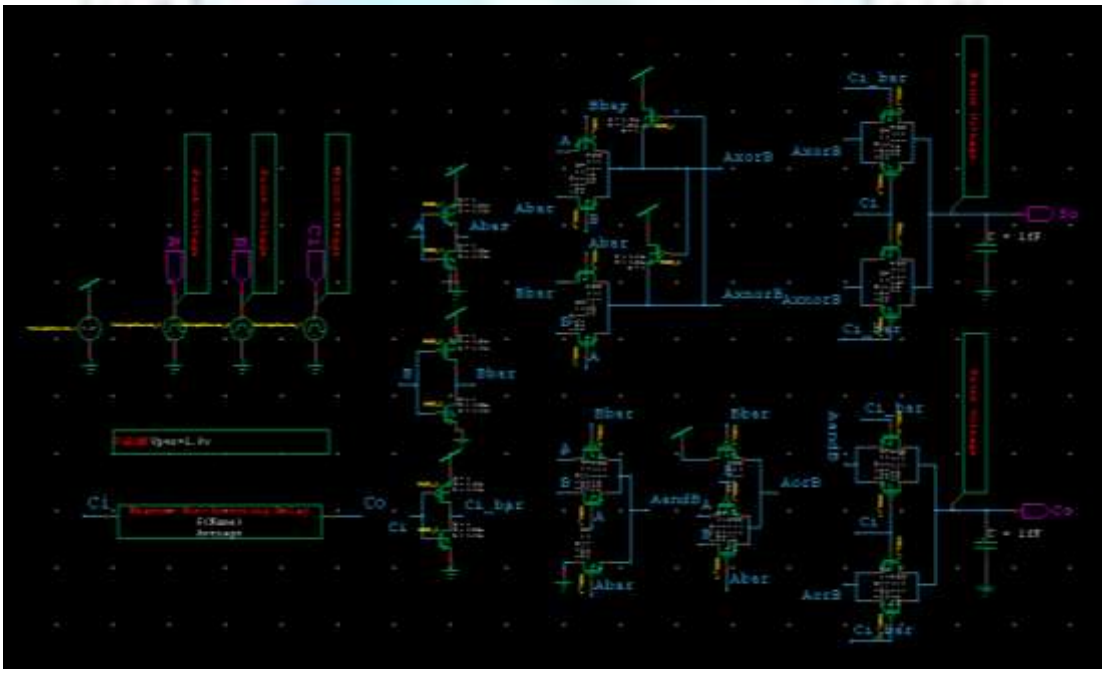

Figure 4. Schematic diagram of SR-CPL FA full adder [7]

While using pass transistors we have to provide a swing restoration logic after whenever we take the output to the next stage. It will raise the voltage level to particularly the high level to Vdd. We can put a weak pMOS transistor and ground it. So, if you do that as you know the voltage level will be pulled to Vdd through weak pMOS transistor, and this is one approach that can be followed, another approach is in addition to this weak pMOS transistor you can put an inverter along with a weak pMOS transistor. The propagation delay for the So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where

the skew between arriving signals is critical for a proper operation, and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications. The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/ NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications [7].

III. PROPOSED HYBRID PTL-TG FULL ADDER

To achieve a good-drivability, low power, high speed and low-energy operations for deep sub micrometer our research is guided to explore hybrid-CMOS style design. Hybrid-CMOS design style utilizes various CMOS logic style circuits to build new full adders with desired performance. This provides the designer a higher degree of design freedom for a wide range of applications. The proposed full adder consists of three modules. Firstly an XOR operation using A and B signals has been performed creating intermediate signals H and H' to be used in the generation of Sum and Carry outputs lately. The Carry generation use transmission gates and Sum generation utilize a combination of pass transistors and transmission gates and Static CMOS.

Co= A.Hbar + Ci.H

So= Ci.Hbar + H.Ci_bar

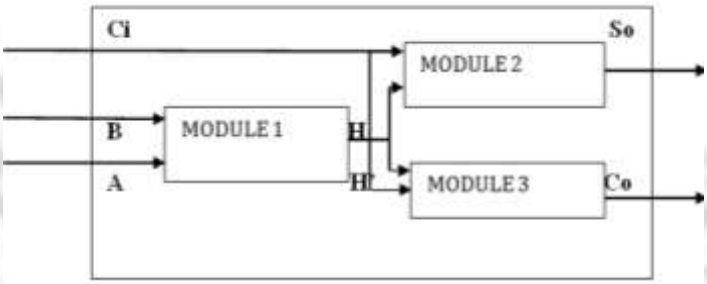

Figure 5. Proposed hybrid full adder Block Diagram

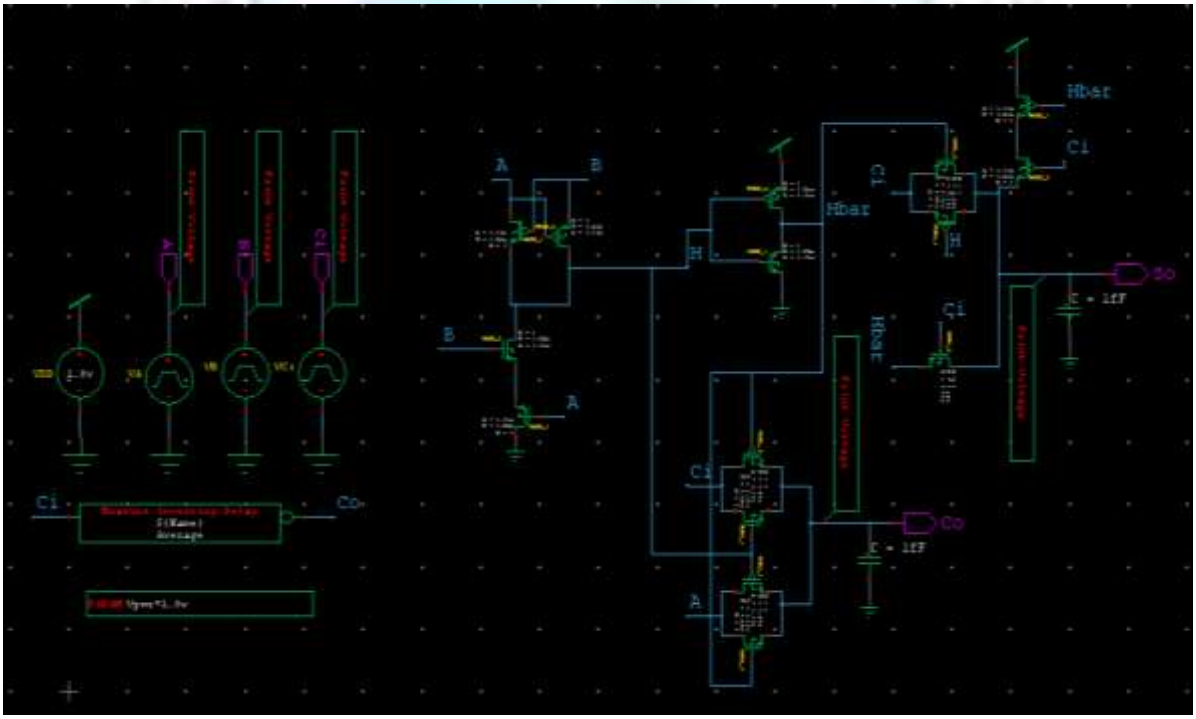

Figure 6. Schematic diagram of proposed hybrid full adder

Module 1: In module 1 Pass transistors and CMOS gates are used for XOR operation of A and B as shown in the schematic and an inverter is used to create the XNOR output.
H = A XOR B
Hbar = A XNOR B = H'

Table 2. Truth table for XOR and XNOR operation

A	B	H=AXOR B	Hbar (AXNOR B)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

It requires 4 transistors (2 nMOS and 2 pMOS) to form H i.e. A XOR B. and two more transistor for inverter. So this module for XOR/XNOR formation requires 6 transistors (3 nMOS and 3 pMOS). This module consumes low power as only 6 transistors are needed. It provides high speed in generation of the XOR signal H and XNOR signal H'. These signal are critical in production of Sum and Carry generation. This module provides good drivability to the adder structure.

Module 2: In module 2, transmission gate and pass transistors are used to form Sum operation. Module 2 uses the signals Ci, H and H' for its operation and it needs 5 transistors for its operation. It is used for module 2 for proposed hybrid adder as it does not suffer from threshold loss problem and it provides full swing outputs. It is a hybrid of pass transistors, Transmission gate and static CMOS network and it provides good alternative for module 2 as it use different logics and provide their advantages and removing their limitations .For example the use of pass transistors allows good drivability and the use of transmission gate provides full swing operation. But when we use longer chains of pass transistors, their performance degrades and needs level restoration and limits full swing outputs. And using only transmission gates in module 2 can lead to low drivability and introduce glitches in the Sum output. But our proposed hybrid structure provides best of all logics in one as each of these design logics complement each other provides best of both results. A capacitive load of 1fF is used for the sum signal.
So = H'. Ci + H. Ci'= Hbar. Ci + H.Ci

Module 3 :
Co= A. Hbar + Ci.H
The module 3 consists of a multiplexer based design of transmission gates . The multiplexer using transmission gates uses two select lines H and H' for its operation and provides Carry output. Transmission gates has the advantage of providing a strong 0 and strong 1 output providing full swing outputs. TG based design of module 3 requires only 4 transistors .So it consumes low power, low area and is relatively faster than other designs of carry logic.
Several logic styles have been used in the past to design full adder cells as stated in literature. Each design style has its own merits and demerits. Classical designs of full adders normally use only one logic style for the whole full-adder design. For example the static CMOS design, Pass Transistor Logic (PTL), Transmission Gate Logic and Complementary Pass Transistor Logic (CPL) etc.

In our work a full Adder cell using PTL (Pass transistor logic) & TG (Transmission Gate) is proposed . TG allows reducing power consumption, propagation delay and low PDP as well. Whereas Pass Transistor Logic (PTL) reduces the count of transistors used, by eliminating redundant transistors and provides good drivability. Other hybrid adders suffers from low output drivability. Our hybrid adder provides not only faster operation and low power consumption as the average power consumed is less and delay is also less .But it provides full swing operation and its operation does not degraded when cascaded structure of our proposed adder is used. It can be seen from the table that the number of transistors in the proposed design are significantly reduced as compared to the reference designs.

IV. RIPPLE CARRY ADDER

The full-adder circuit presented here can be used as the basic building block of a general n-bit binary adder, which accepts two n-bit binary numbers as input and produces the binary sum at the output. The simplest such adder can be constructed by a cascade connection of full adders, where each adder stage performs a two-bit addition, produces the corresponding sum bit, and passes the carry output on to the next stage. Hence, this Cascade adder configuration is called the carry ripple adder. The overall speed of the carry ripple adder is obviously limited by the delay of the carry bits rippling through the carry chain; therefore, a fast carry-out response becomes essential for the overall performance of the adder chain [2].
A 2 Bit ripple carry adder is designed. A0, B0, C0 are the three inputs to the first adder and S0, C1 are its outputs. C1 passes to the 2^{nd} adder and A1,B1 are the other two inputs and C2 is the output Carry and S1 is the output sum of second adder.

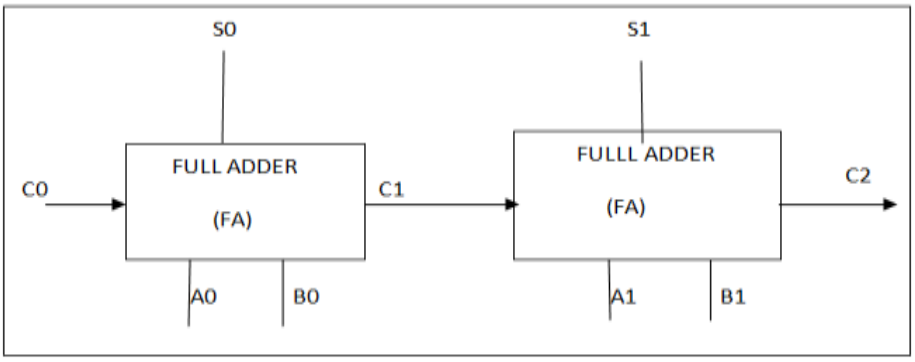

Figure 7. 2 bit-ripple carry adder

2-bit ripple carry adder using proposed hybrid full adder

2 bit ripple carry adder using the proposed full adder using TANNER EDA is shown in the figure7. For reduction of complexity we have taken inputs as A0=A1, B0=B1. A0, B0, C0 are the inputs of the first adder and S0, C1 are the sum and carry outputs. A1, B1,C1 are the inputs of the 2nd cascaded adder S1 and C2 are the sum and carry outputs. Average power dissipated and propagation delay between C0 and C2 has been measured.

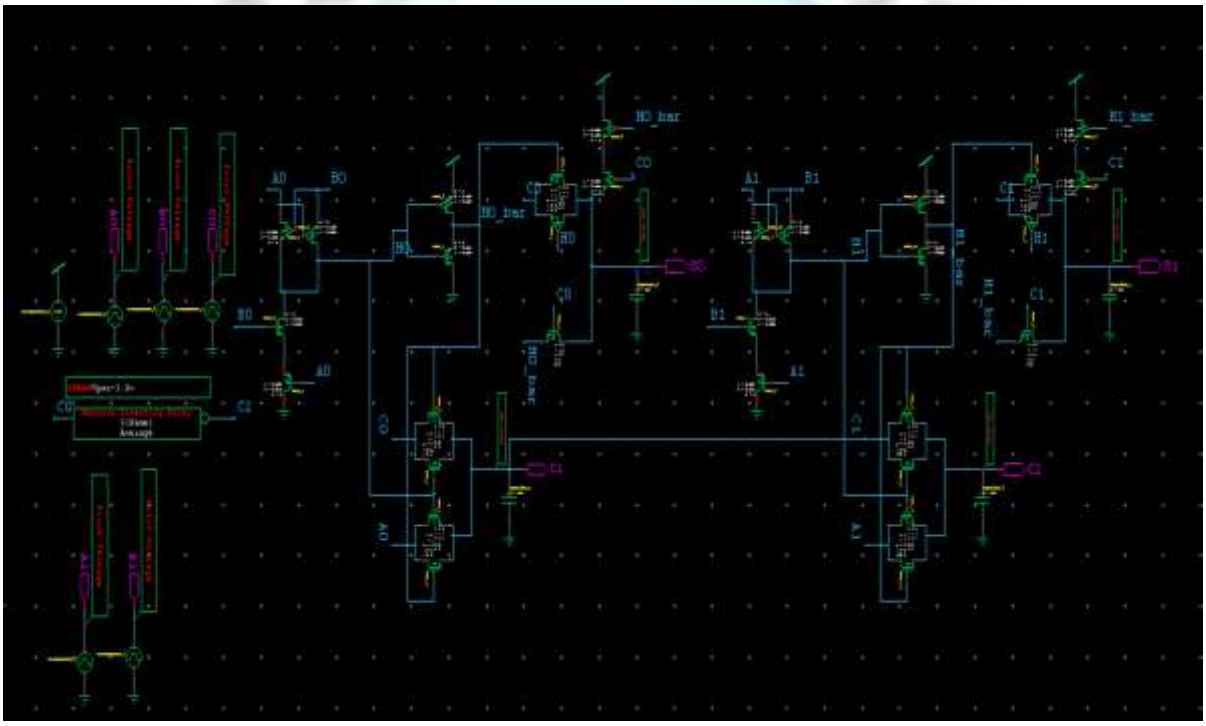

Figure 8. Schematic diagram of 2 bit ripple carry adder using proposed adder

V. SIMULATIONS AND RESULTS

Simulation of various adder structures have been done using TANNER EDA v14 tool using CMOS 180 nm technology .The W/L ratio of NMOS and PMOS is 250nm/180nm and 500/180 nm respectively for all adder cells .The W/L ratio of PMOS is double of NMOS as PMOS transistors are slower in comparison to NMOS transistors. And the average power dissipation and total propagation delay of the carry signal, Power Delay Product has been measured with variation of the supply voltage and Vdd and results are given in table 3,4,5. It has been observed that in case of Proposed PTL-TG full adder the average power, delay and Power Delay Product is smaller than the existing DPL and SR-CPL full adders that were reported in[7]. The tables 6,7,8 show the power, delay and PDP results of the existing adders in paper[7] and * shows our implementation of existing adders and our proposed PTL-TG hybrid adder at 200

MHz frequency,1.8V supply voltage and 1fF load. The comparative results are shown in figure 11,12,13. A ripple carry adder is also designed using proposed adder under same load conditions.

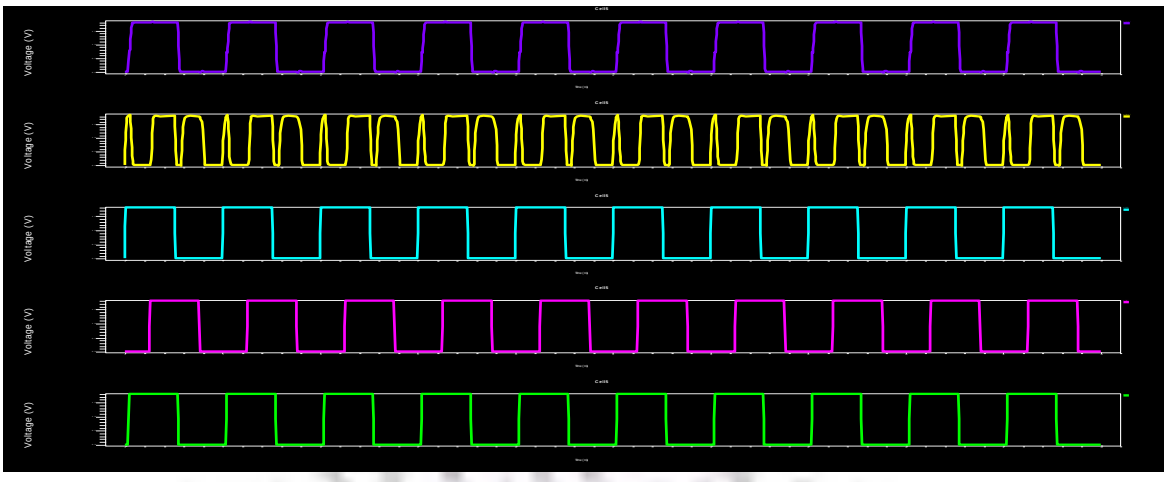

Figure 9. W-Edit waveform for the proposed PTL-TG Hybrid full adder

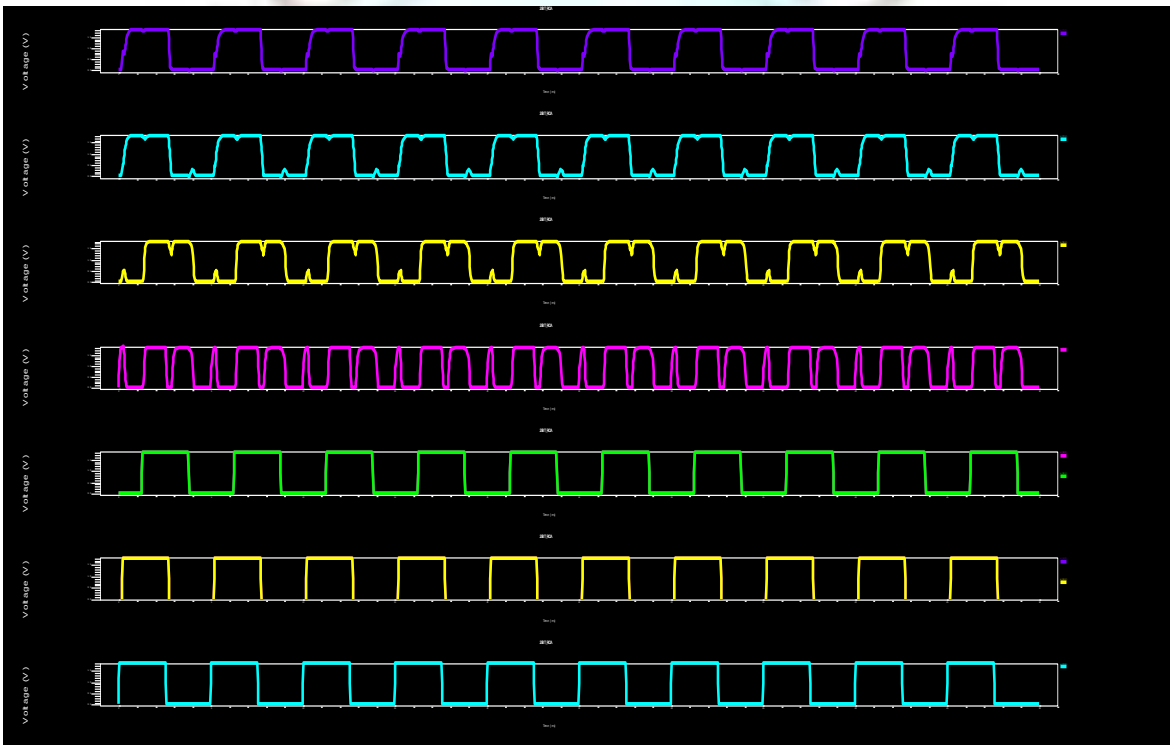

Figure 10. W-EDIT waveform for 2-bit ripple carry adder

Table 3: Variation of Average power with supply voltage at f=200MHz.

Supply voltage	DPL-FA	SR-CPL FA	Proposed PTL-TG Hybrid FA
1.2V	22.719 µW	22.657 µW	12.573 µW
1.4V	31.535 µW	30.164 µW	17.058 µW
1.6V	40.782 µW	38.455 µW	22.600 µW
1.8V	52.126 µW	48.733 µW	28.707 µW

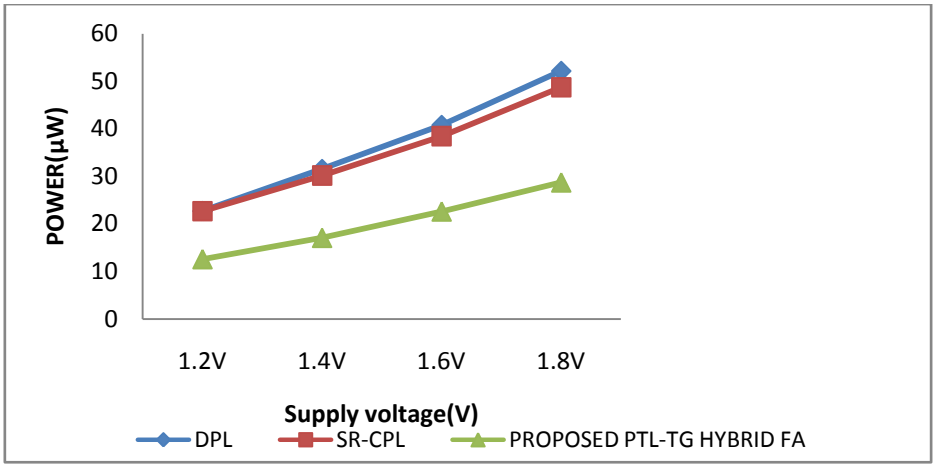

Figure 11. Variation of Avg. power dissipation (µW) with supply voltage at f=200MHz

Table 4: Variation of delay with respect to power supply at f=200MHz.

Supply voltage	DPL-FA	SR-CPL FA	Proposed PTL-TG Hybrid FA
1.2V	403.63 ps	351.65 ps	296.72 ps
1.4V	339.53 ps	312.96 ps	258.47 ps
1.6V	309.47 ps	292.97 ps	245.74 ps
1.8V	267.18 ps	272.10 ps	234.2 ps

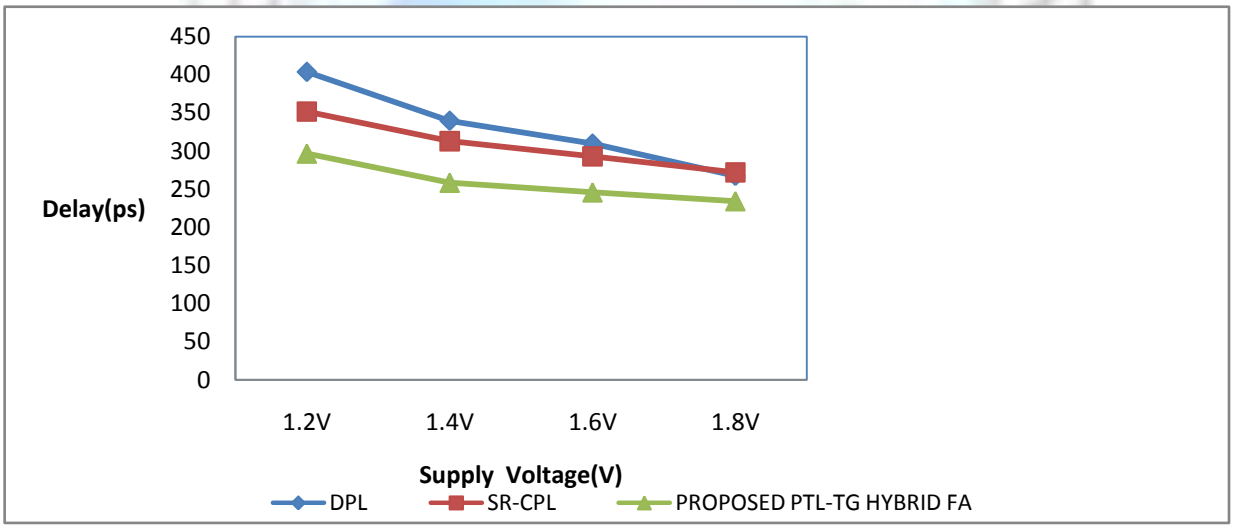

Figure 12. Delay with respect to supply voltage at f=200MHz.

Table 5. Variation of PDP of various adders with supply voltage at f=200MHz.

Supply voltage	DPL-FA	SR-CPL FA	Proposed PTL-TG Hybrid FA
1.2V	**9.170 fJ**	**7.967 fJ**	**3.730 fJ**
1.4V	**10.707 fJ**	**9.440 fJ**	**4.408 fJ**
1.6V	**12.620 fJ**	**11.266 fJ**	**5.553 fJ**
1.8V	**13.927fJ**	**13.260 fJ**	**6.723 fJ**

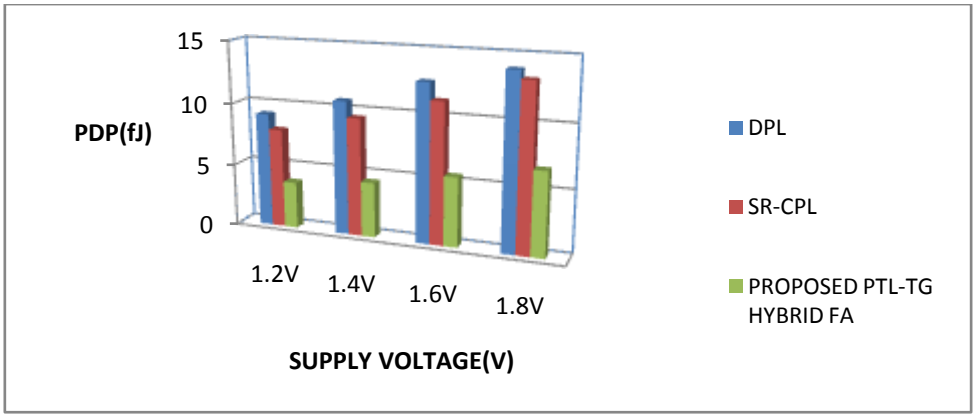

Figure 13. Variation of PDP (fJ) with supply voltage at f=200MHz.

Table 6.Comparison of power of existing and proposed adder

Average power(µW)					
ADDER	**EXISTING DPL FA**		**EXISTING SR-CPL FA**		**PROPOSED ADDER**
Supply voltage(V)	**In paper[7]**	**Our Implementation**	**in paper [7]**	**Our Implementation**	
1.8V	55.1 µW	52.12 µW *	60.6µW	48.73 µW*	28.707µW

Table 7. Comparison of Delay of existing and proposed adder

Delay in picoseconds					
ADDER	**EXISTING DPL FA**		**EXISTING SR-CPL FA**		**PROPOSED ADDER**
Supply voltage(V)	**In paper[7]**	**Our Implementation**	**in paper [7]**	**Our Implementation**	
1.8V	289 ps	267.18 ps*	278 ps	272.10 ps*	234.2 ps

Table 8. Comparison of PDP of existing and proposed adder

Power Delay Product (fJ)					
ADDER	**EXISTING DPL FA**		**EXISTING SR-CPL FA**		**PROPOSED ADDER**
Supply voltage(V)	**In paper[7]**	**Our Implementation**	**in paper [7]**	**Our Implementation**	
1.8V	15.9 fJ	13.927 fJ	16.8fJ	13.260 fJ	6.723 fJ

Conclusion

Simulations of various adders have been performed using TANNER EDA v14. In simulation work , First of all Schematics of various adders were created using Tanner's S-edit , then spice netlists were created and analyzed using T-Spice module of the software. Then Waveforms and output files obtained using W-edit. Power and delay are the two main performance parameters in the thesis work. Power, Delay and PDP of our proposed adder shows significant improvement at different supply voltages and frequencies. It is observed that the proposed adder shows 47.9%, 19.03% , 57.7 % improvement in power , delay and PDP as compared to existing DPL-FA in paper[7]. And the proposed adder shows 52.6%, 15.75%, 59.98 % improvement in power , delay and PDP as compared to existing SR-CPL FA in paper[7]. At 1.8 V supply voltage and 200 MHz frequency, the proposed hybrid adder exhibits Average power dissipation, delay and power delay product are 28.707 µW, 234.2 pico- seconds and 6.723 fJ respectively. The 2 bit ripple carry adder is formed using the purposed adder which provides low power and high speed operation .It can be used for longer cascaded adder chains for arithmetic application

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