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# A Review of Various Low Power SAR Based ADC Architectures

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**ABSTRACT**

**Analog-to-digital converters (ADC) targeted to be used in medical implant devices serve a vital role because the interface between analog signal and digital process system. Usually, low power consumption is needed for a protracted battery life. In such application which needs low power consumption and moderate speed and resolution, one among the foremost frequently used ADC architectures is that the successive approximation registers (SAR) ADC. In this paper, we have presented a review of various ADCs, which will help the researchers to carry forward their research in this field effectively.**

**Keywords: Analog-to-digital converter (ADC), charge redistribution, CMOS, low power, low supply voltage, successive approximation, latched comparator**

## 1. INTRODUCTION

As signal processing is broadly used in various fields, such as audio, control, communication and medical systems, the problem of dealing with both analog signal and digital signal becomes prevalent. Data converters serve a role as the interface between the analog and digital world. Figure1 describes a basic signal processing system. The analog input signal is first filtered to remove high-frequency components in order to avoid aliasing. Then the signal is sampled at frequency $f_S$, and the discrete sampled data is digitized in the analog-to-digital converter (ADC). The digital outputs from ADC are executed in the digital signal processor (DSP). Finally, they return to an analog signal by the conversion of digital-to-analog converter (DAC) and removal of unevenness by the followed reconstruction filter.

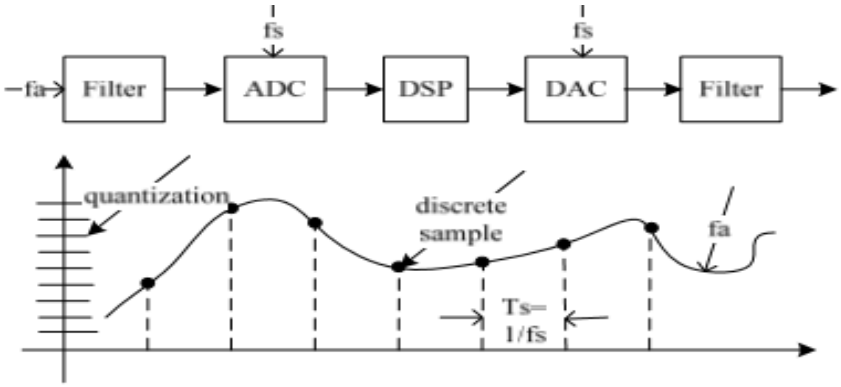


**Figure 1 Basic signal processing system**

## 2. GENERAL CHARACTERISTICS OF ADC

**Resolution:** The resolution of an ADC is the number of its output words, which shows the minimum input voltage that an ADC can produced a code transition. The smallest step is explained as the least-significant-bit (LSB) by equation $V_{LSB} = V_{REF}/2^N$, where $V_{REF}$ is the reference voltage of the converter.

**Aliasing:** When a discontinuous analog signal is sampled, it becomes a discreet signal. The sampling frequency should be at least two times greater than the signal frequency; otherwise, aliasing will take place. This rule is known as Nyquist Criterion. Figure 2 shows an example of aliasing caused by improper sampling frequency. It may cause in another different frequency and keep it hard to recover from the original one

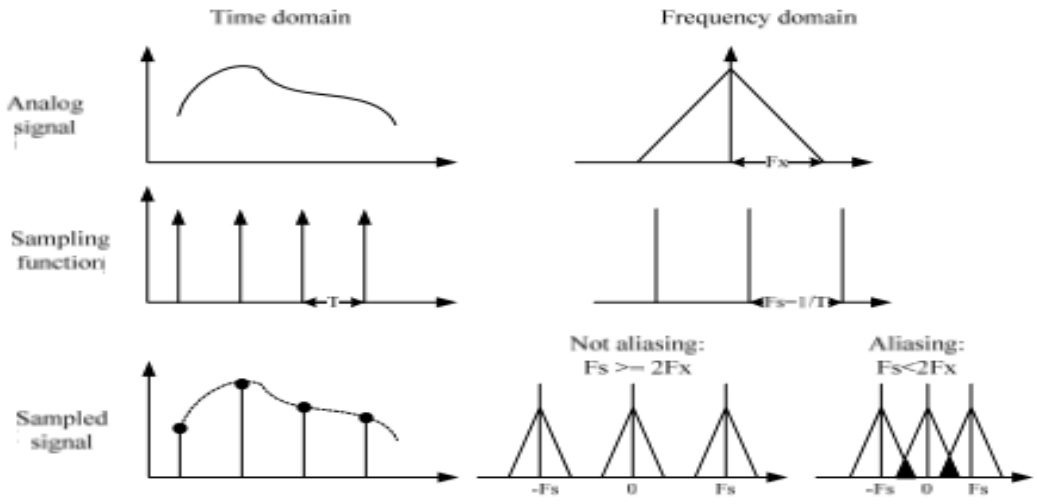


**Figure 2 Explanation of aliasing in the time and frequency domain**

**Quantization Error:** ADC changes the analog signal to certain extents. The infinite analog information is converted to limited digital codes. During the quantization, even ideal ADC generates error, known as quantization error. At the initiation of each code transition, there is no error. As the analog signal enhances, the error also becomes greater. The maximum error here is 1LSB (Δ).

## 3. ADC ARCHITECTURES

**Flash ADC:** Flash ADC is known for its quick speed. As described in Figure 3, it has $2^N$-1 comparators corresponding to $2^N$-1 quantization steps. The total $2^N$ resistors generate all the voltage references. The comparator output is one if the input voltage is greater than the related reference voltage, and zero vice versa. There is a decoder follows at the last stage to interpret the thermometer code generated by comparators to N-bit binary digital output.

Though Flash ADC has a high speed, the great numbers of comparators consume immense power and area. Taking a 9-bit Flash ADC as an example, there will be 511 comparators in the circuit. This liability limits the resolution of Flash ADC up to 6 bits

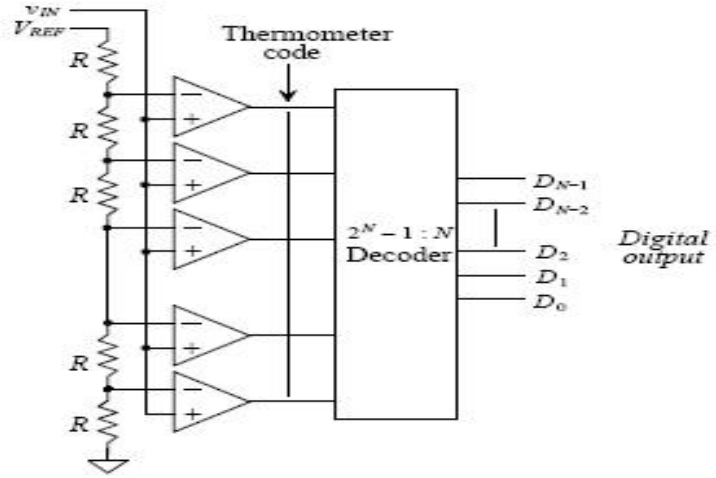


**Figure 3 Block diagram of a Flash ADC**

**Pipeline ADC:** Same as the operation of the Ist stage, the amplified residue is again sampled and compared with $V_{ref}/2$. The above operation continues until the LSB is determined. Pipeline ADC requires N clock cycles to complete the first conversion, but afterwards it can do each conversion per clock cycle because of its property of pipelining .Though Flash ADC has a high speed, the great numbers of comparators consume immense power and area.

**Integrating ADC:** Integrating ADC, as its name shows, integrates the input signal and counts the integration time. The counted time changed to N-bit digital information. A popular type of converter based on this theory is the dual slope converter . Before the depiction of the dual slope converter will consider on single slope converter. It is the simple and basic type of integrating ADC. The single slope converter composed of an integrator, a comparator and a counter. Before the integration starts, the input voltage is sampled ($V_{IN}$) and the integrator is reset by closing the switch. Then

$V_{IN}$ is hold and sent to the comparator. At the same time the integrator starts producing the ramp function and the counter starts countering clock pulses. The moment the integrated voltage ($V_C$) is greater than $V_{IN}$, the counter stops.

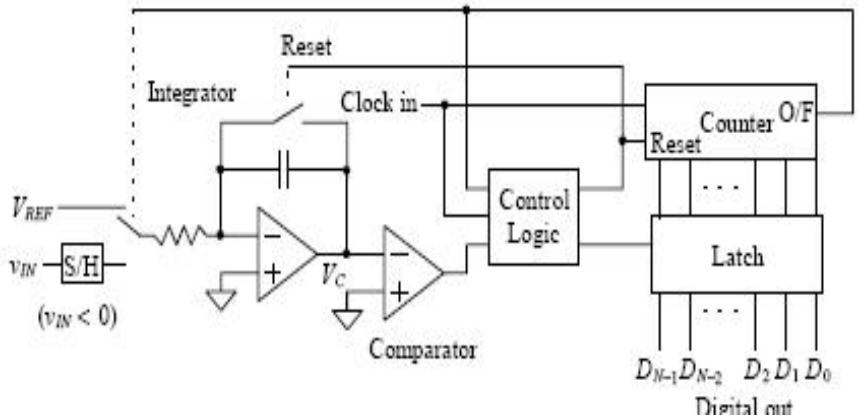


**Figure 4 Block diagram of a dual slope ADC**

**Successive Approximation Register ADC:** SAR ADC is based on a binary search algorithm. It is composed of a successive approximation register (SAR), a digital-to-analog converter, a comparator and a sample and hold circuit, which is shown in Figure 5. Firstly, input voltage ($V_{IN}$) is sampled and the registers are reset to zero. Secondly, the conversion begins by an approximation of MSB (set MSB as 1) by SAR; DAC changes the digital information to a voltage $V_{OUT}$ (half of the reference voltage $V_{REF}$); Comparator compares $V_{OUT}$ with $V_{IN}$. If $V_{IN}$ is greater than $V_{OUT}$, it outputs one, otherwise, it outputs zero; SAR loads the comparator result, store the value of MSB and produces its next approximation; the conversion continues until the LSB is determined. Therefore, an N-bit SAR ADC needs N clock cycles per conversion.

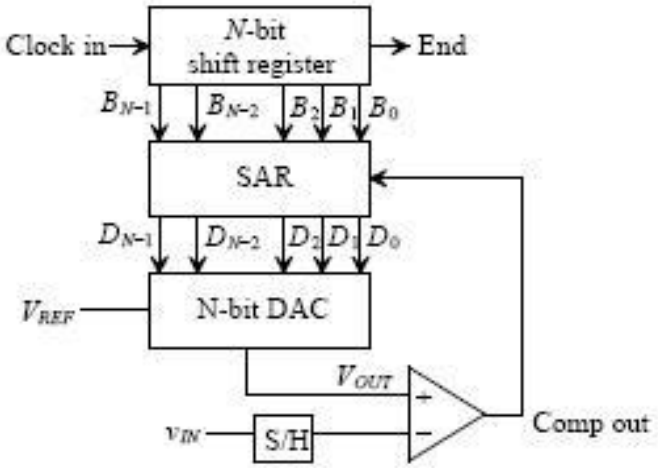


**Figure 5 Block diagram of a SAR ADC**

SAR ADC is popular for its simple structure, thus consumes less power and saves greater die size. Yet, with enhancement of its resolution, the linearity problem of DAC becomes more terrible, which directly results non linearity of ADC. Hence, SAR ADC is not appropriate for high resolution.

## 4. ADC PERFORMANCE METRICS

**Static Performance:** Static errors are divergence of conversion transfer characteristics from ideal one. The static performance of an ADC is described by these metrics: offset error, full-scale error, differential nonlinearity, integral nonlinearity and missing code.

**a) Offset Error and Full-Scale Error**: Offset error is the difference between the Ist code transition point and the ideal one; Full-scale error is the difference between the last code transition point and the ideal one.

**b) Differential Nonlinearity (DNL):** Differential nonlinearity is the difference between the ideal code width of 1LSB and the actual code width.

**c) Integral Nonlinearity (INL):**Integral nonlinearity is the difference between the actual code transition point and that of the ideal code transition. Moreover, INL is found equal to the accumulative sum of DNL [5].

**d) Missing Codes:** when the analog input enhances from zero to the full-scale value, not all the digital output codes are produced. This is known as missing codes.

**Dynamic Performance:** Static error is examined by DC signal, and it does not involve any information about noise and high frequency results. Opposite to static error, dynamic error is examined with periodic waveform, which gets extra information of ADC performance, such as SNR, SINAD, SFDR and ENOB

**a)Signal-to-Noise Ratio (SNR)**: For an ideal ADC, signal-to-noise ratio (SNR) is the ratio of an RMS (root mean square) full-scale input to its RMS quantization error [11].

**b) Signal-to-Noise-and-Distortion Ratio (SINAD)**: Signal-to-noise-and-distortion ratio (SINAD) denotes the value of the input signal amplitude over the rms sum of all rest spectral components .

**c) Spurious-Free Dynamic Range**: A Spurious-free dynamic range (SFDR) is the value of the input signal to the greatest spur, which is generally a harmonic of the input tone.

**d) Effective Number of Bits**: Effective number of bits (ENOB) is often used in place of the SINAD. It is often used to indicate ADC accuracy at a specific input frequency and sampling rate [11].

## 5. COMPARISON

ADCs are selected according to specific requirements on considering the resolution, power, size, sampling frequency, performance and etc. For some applications, almost all the architectures may work well; for rest, there may be a better choice to gain the best result. For example, a Flash ADC is most famous for applications requiring ultra-high speed when power consumption is not main concern; A Sigma-Delta ADC is always the best choice when high resolution is needed; A SAR ADC is generally first considered to obtain low power and small size with medium resolution[7][8].

**Table I Classifications of 3 types of ADCs [9]**

| Performance | ADC | Low Resolution (8-13 bits) | Medium Resolution (14-19 bits) | High Resolution (>=20 bits) |
|---|---|---|---|---|
| Sample Rate | Sigma-Delta | N.A. | 128S/s - 100kS/s | 15S/s - 625kS/s |
| | SAR | 20kS/s - 4MS/s | 40kS/s - 4MS/s | N.A. |
| | Pipeline | 2MS/s - 550MS/s | 1MS/s - 400MS/s | N.A. |
| Power | Sigma-Delta | N.A. | 0.3mW - 245mW | 0.3mW - 600mW |
| | SAR | 0.25mW - 225mW | 1.95mW - 413mW | N.A. |
| | Pipeline | 15mW - 2250mW | 250mW - 1900mW | N.A. |

Table I illustrates a category of three most famous ADC architectures available these days in terms of resolution, power and sample rate. The idea of categorized is referred to [10] and the data is based on [9]. The three architectures (Sigma-Delta, SAR and Pipeline ADC) have been broadly studied these days because of the burning topic of low-power and low-voltage applications. Though the data illustrates here is not an absolute presentation of the exact performance that these ADCs can gain, it is at least a rough and quick reference based on the information given by manufacturers' guide [9]. For example, when it comes to medium resolution, if speed is the priority, Pipeline ADC can be the better choice due to its high sample rate. However, if the power consumption is the priority, SAR or Sigma-Delta ADCs can be chosen.

## CONCLUSION

In this paper, we have presented a review of various ADCs. In order To minimize power, in ADC a capacitive DAC with S/H circuit along with a binary-weighted capacitor array for the DAC is used. Further we have compared and analyzed different topologies of comparator. A transmission gate (also called CMOS switch) is preferred both for its relatively constant on-resistance and charge injection cancellation to optimize the choice in terms of low power and medium resolution and speed among the ADC architectures.

## REFERENCES

[1]. L. S. Y. Wong, et al., "A Very Low-Power CMOS Mixed-Signal IC for Implantable Pacemaker Applications," IEEE Journal of Solid-State Circuits, vol. 39, no. 12, pp. 2446-2456, Dec. 2004.
[2]. Analog Device, Mixed-Signal and DSP Design Techniques, Newnes, 2003
[3]. S. Mortezapour and E. K. F. Lee, "A 1-V, 8-bit Successive Approximation ADC in Standard CMOS Process," IEEE Journal of Solid-State Circuits, vol. 35, no. 4, pp. 642–646, 2000
[4]. J. L. Mccreary and P. R. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part 1," IEEE Journal of Solid-State Circuits, vol. sc-10, no. 6, Dec., 1975.
[5]. M. D. Scott, B. E. Boser and K. S. J. Pister, "An Ultralow-Energy ADC for Smart Dust," IEEE Journal of Solid-State Circuits, vol. 38, no. 7, July, 2003
[6]. K. Abdelhalim, L. MacEachern, and S. Mahmoud, "A Nanowatt Successive Approximation ADC with Offset Correction for Implantable Sensor Applications," in Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on, 2007, pp.2351-2354.
[7]. G. Promitzer, "12-bit Low-Power Fully Differential Noncalibrating Successive Approximation ADC with 1MS/s," IEEE J. Solid-State Circuits, vol. 36, no. 7, pp. 1138–1143, July, 2001.
[8]. N. Vermna and A. p. Chandrakasan, "A 25µW 100kS/s 12b ADC for Wireless Micro-Sensor Applications," ISSCC Dig. Tech. Papers, pp. 222-223, Feb. 2006.
[9]. M. v. Elzakker et al., "A 1.9µW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," ISSCC Dig. Tech. Papers, pp. 244-245, Feb. 2008.
[10]. B. P. Ginsburg and A. P. Chandrakasan, "Dual Time-Interleaved Successive Approximation Register ADCs for an Ultra-Wideband Receiver," IEEE J. Solid-State Circuits, vol. 42, no. 2, pp. 247–257, Feb, 2007.
[11]. Y. S. Yee, L. M. Terman, and L. G. Heller, "A Two-Stage Weighted Capacitor Network for D/A–A/D Conversion," IEEE Journal of Solid-State Circuits, vol. SC-14, pp. 778–781, August 1979
[12]. K. S. Tan at el., "Error Correction Techniques for High-Performance differential A/D Converters," IEEE Journal of Solid-State Circuits, vol.25, no. 6, pp. 1318-1326, Dec, 1990.
[13]. T. O. Anderson, "Optimum Control Logic for Successive Approximation Analog-to-Digital Converters," Computer Design, vol. 11, no. 7, pp. 81–86, 1972
[14]. J. L. Mccreary and P. R. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part 1," IEEE Journal of Solid-State Circuits, vol. sc-10, no. 6, Dec., 1975.