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Phase Locked Loop

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ABSTRACT

Here we look into different topologies of phase locked loop which allows Q-dot device to be used in Mixed-signal design and low power BJT in RF front end design from Mathematical point of view. We found the phase detector, a mixer and different implementation of loop filters. We expect the PLL to be of low power, faster and less jittery.

1.0 INTRODUCTION

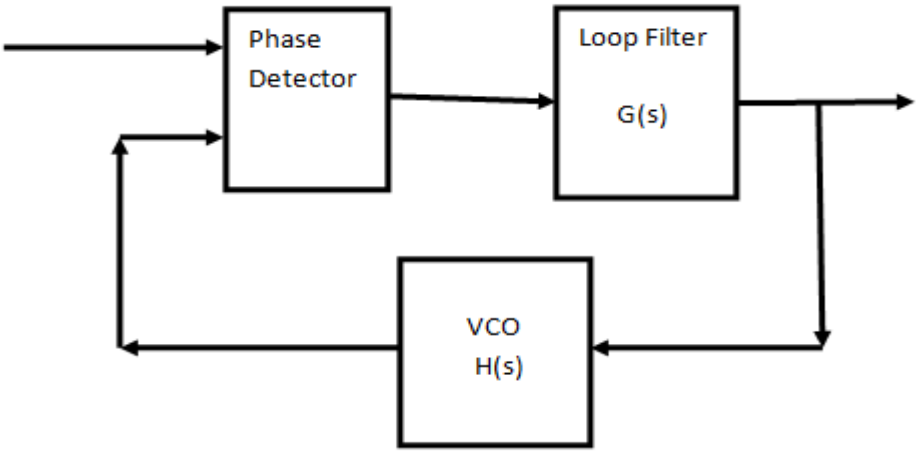
A phase locked loop (PLL) allows a particular system to track another system. It is extensively used in carrier recovery of communication systems, in mobile handsets and base station, in Global Positioning System (GPS), in computer to generate jitter free clock and in Data recovery from hard disk in computer or DVD. The PLL is in use since 1920s for synchronous receiver of FM/AM modulation and in television receiver. Here we are looking at the usage of PLL for mixed signal applications and RF down conversion.

The detailed analysis and uses of PLL is discussed in reference [1] and [2], which is avoided here. A PLL contains three basic blocks: a phase detector, a loop filter and a voltage controlled oscillator (VCO)[3] and [4]. When the loop is locked, the control voltage generated out of loop filter is such that the VCO frequency is equal to the average of the input frequency. To maintain the control voltage we need an extra integrator to give a better performance against noise which has a constant even when the loop filter output is zero. Thus we have simpler loop filter.

The organization of this paper is as follows. The section II introduces the basic topology of phase locked loop. The section III and IV introduce innovations required in the phase detector and mixer to dissipate less power. The section V and VI discuss the innovation in the loop filter and the Voltage controlled oscillator (VCO) for using Q-dot device. The section VII deals with the schematic diagram for mixed signal application. We conclude the paper in the next section.

2.0 BASIC TOPOLOGY

The phase detector is implemented by a using XOR gate [2]. The loop filter is very important in deciding the speed and accuracy of PLL. It is given as G(s) in Figure 1 which is a low pass filter of different transfer functions.



Fiegure 1: Phase locked loop.

The VCO is normally implemented by charging of capacitor by current, found proportional to the controlled voltage. Hence it has a transfer function of K_o/s which is given as H(s). The phase detector works as the subtractor in phase in closed loop provides a negative feedback. Thus the closed loop transfer function will be given as G(s)/[1+G(s)H(s)] which should have all its pole in left half plane in root locus plot for a given K_o for stable operation.

In Q-dot technology, we may vary the capacitance or steer away the current. Both cases it will provide an integration of the controlled voltage.

3.0 INNOVATION IN PHASE DETECTOR

For the phase detector, a number of logical circuits may be used like XOR gate, J-K flip/flop etc [2]. Figure 2 shows the XOR implementation in Q-dot circuit. We find that the charges or ion pulsate between two capacitor if not dissipated in the Q-dot device, hence consumes less energy.

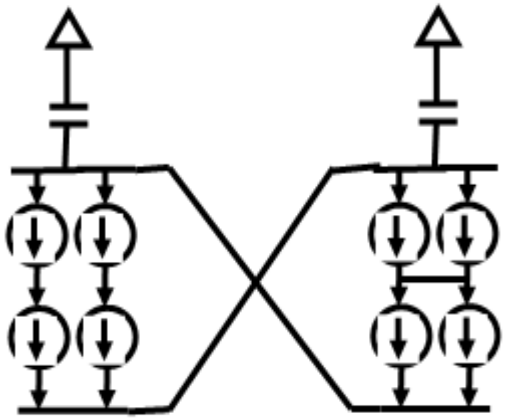


Figure 2. XOR gate: gate signals are (V-in,&CLK_bar)or(V_in_bar& CLK);(V_in or CLK_bar)&(V_in_bar or CLK).

The phase detector shows zero phase error (actually a signal of twice the frequency) if the input signal and the clock is 90 degree out of phase. Figure 3 shows the averaged phase detector output in case the signal is bounded between 0 volt to U_{max} volt. It will be triangular shaped graph bounded between +/-Umax/2 across its average value.

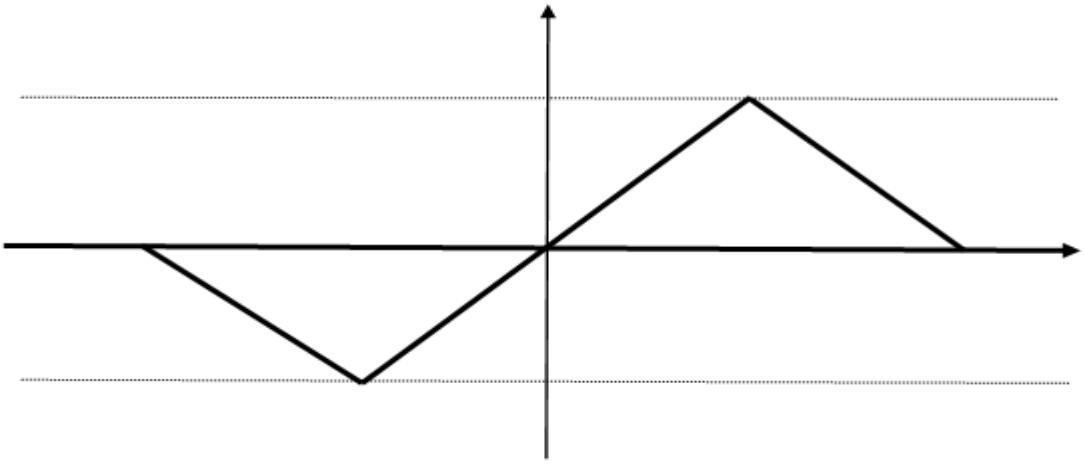


Figure 3. Plot of averaged phase detector output.

We use phase detector for digital phase locked loop which means that the signals to the PD are square waves. This is used in clock generation in computer, cell phone and all other digital/mixed signal VLSI circuits. When it is locked the signals should be 90 degree out of phase to guarantee proper functioning of the circuit.

4.0 INNOVATION IN MIXER

In down conversion of radio frequency signal in cell phone, radio, television we need mixer which works as two quadrant multiplier of two input signals sinusoidal in nature. This could be frequency-shift-keyed (FSK), phase-shift-keyed or pulse

amplitude modulation (PAM). Our goal is to use a Q-dot/QFET circuit which could be modified from XOR gate Q-dot circuit and used as analog multiplier. The circuit found here, is a modified Gilbert cell using BJT as shown in Figure 4 and explained below.

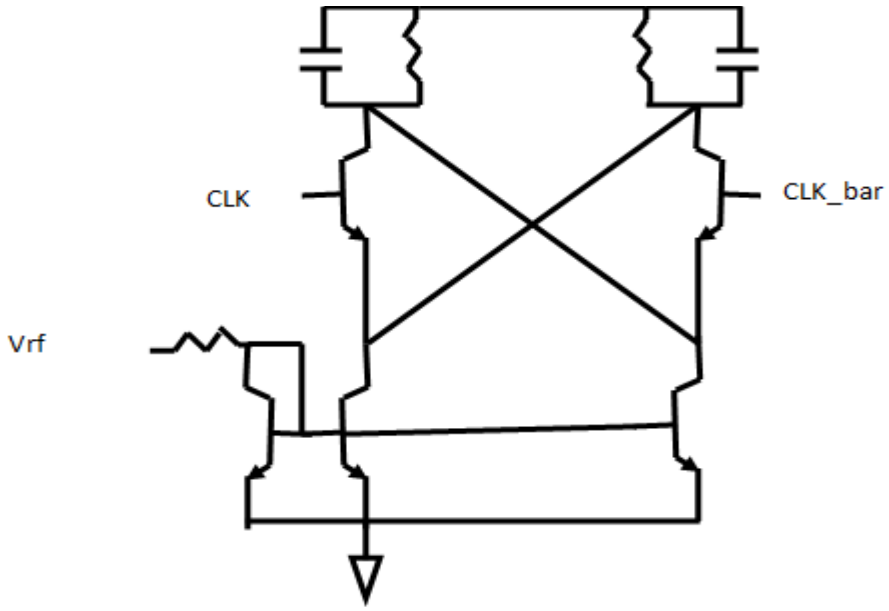


Figure 4. Modified Gilbert Cell for 2 quadrant mixer.

Here the input RF signal is given at the current source and the clock signal from VCO is given to the middle two transistors in Gilbert cell. We put two capacitors across two resistors and cross couple the emitter to the collector of the other transistor. The collector current will be $I_{c1}= I_{EE}*\exp(V_i/V_T)$ and $I_{c2}= I_{EE}*\exp(-V_i/V_T)$. The current difference pulsates between two capacitors without getting dissipated in resistor. The I_{EE} is proportional to the RF voltage.

5.0 INNOVATION IN LOOP FILTER

In most analog PLL, the loop filter is implemented by resistor and capacitor of different forward loop transfer function, like $1/(s+a)$ or $1/s(s+a)$ or $1/(s^3+as^2+bs)$ [6][7]. They are implemented as shown in Figure 5.

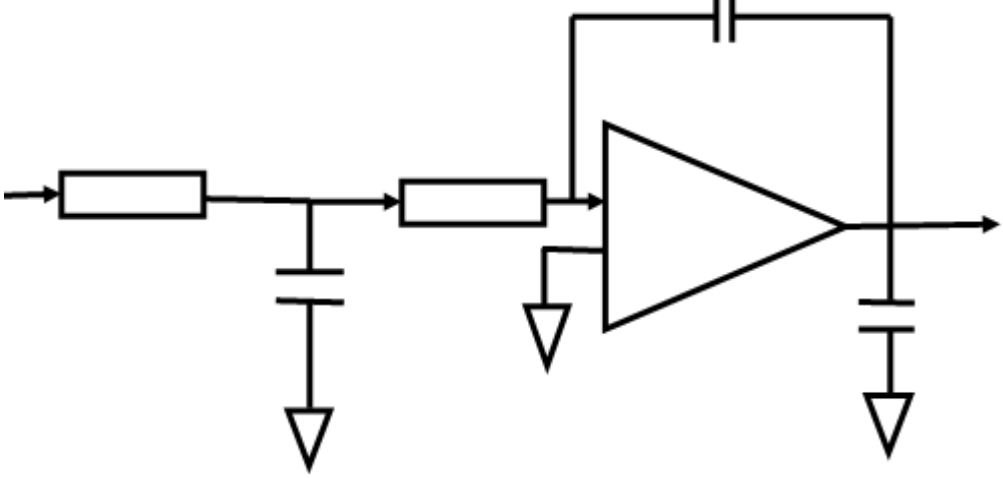


Figure 5. Second order loop Filter.

The overall transfer function will be $G(s)/[1+G(s)H(s)]$ and to maintain stability the poles should be in the left hand plane. We can find the gain in closed loop K_o by using Routh's stability criterion [5].

Now a close look into the loop filter in Figure 5, shows that in some cases, K_o/s will be K_o thus allowing a second order closed loop transfer function.

6.0 INNOVATION IN VCO

The oscillator circuit using Q-dot device is given in reference [8]. We can convert it to voltage controlled oscillator using current steered method or by changing the capacitor value. Here we show the second method in Figure 6. This circuit is oscillatory and uses low power dissipation.

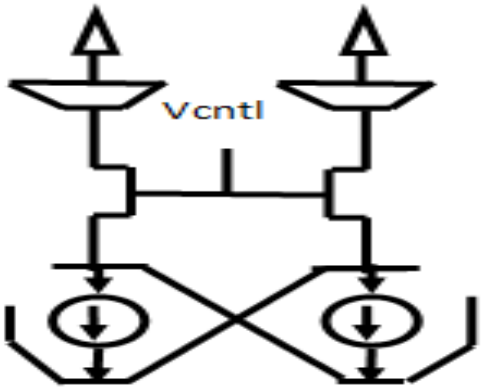


Figure 6. Voltage Controlled Oscillator.

We have talked about PLL for mixed signal purpose. We normally use a charge-pump for mixed signal PLL, but here we use them as normal PLL with phase detector.

7.0 SCHEMATIC DIAGRAMS

From Figure 1, we know the components required in a PLL. These components are described separately, but in schematic we connect them. Here there is difference of a differential low gain amplifier stage which provides a high impedance node. The schematic is yet to be tested, hence this paper is a proposal for a mixed signal/RF PLL. The schematic is shown in Figure 7.

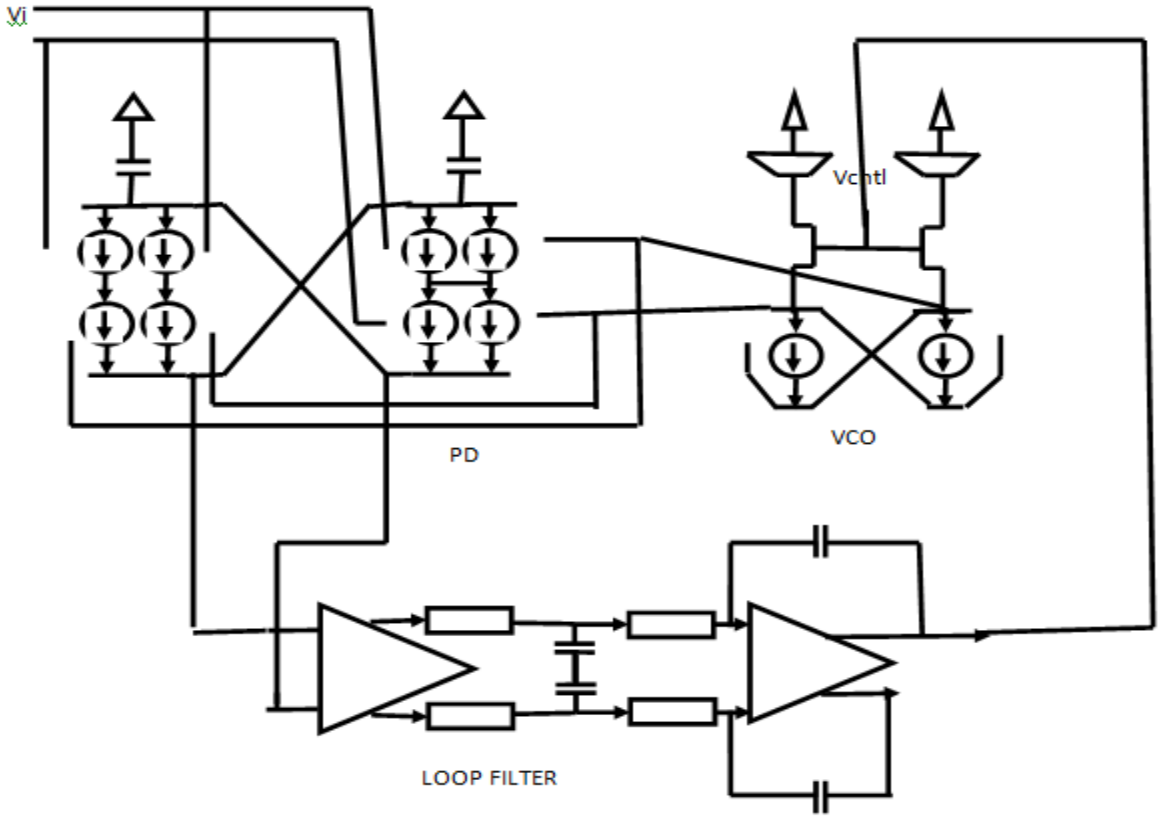


Figure 7. Schematic for mixed signal PLL without charge pump.

CONCLUSION

Here we have described a method of implementing mixed signal PLL using Q-dot device. We use XOR as phase detector, a second order loop filter and a VCO with voltage controlled capacitor. We expect it to work better than CMOS PLL in a sense that it will consume less power. The VCO gain is the deciding factor in determining the jitter as well as its tracking capability of input signal.

REFERENCES

[1]. F M Gardner, "Phaselock Techniques," John Wiley & Sons, 2nd Edn.
[2]. R E Best, "Phase-Locked Loop," McGraw-Hill, 3rd Edn.
[3]. P R Gray, R G Meyer, "Analysis and Design of Analog Integratd Circuits," John Wiley & Sons, Inc., 3rd Edn.
[4]. R E Ziemer, W H Tranter, "Principle of Communications, System Modulation and Noise," John Wiley & Sons, 5th Edn.
[5]. K Ogata, "Modern Control Engineering," Prentice-Hall of India Pvt. Ltd., 2nd Edn.
[6]. A K Dutta, "GPS Receiver," International Journal of Enhanced Research in Science Technology & Engineering, ISSN 2319-7463 Vol. 5 Issue 1, January-2016
[7]. A K Dutta, "Optimum Detection of CDMA," International Journal of Enhanced Research in Science Technology & Engineering, ISSN 2319-7463 Vol. 5 Issue 3, March-2016
[8]. A K Dutta, "UHF RF Transmitter and Receiver," International Journal of Enhanced Research in Science Technology & Engineering, ISSN 2319-7463 Vol. 3 Issue 11, November-2014