

# Comparison of SRAM cells at different-2 technology

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**Abstract:** This paper represents of simulation of SRAM Cells with load (6T) and without load (4T) and their comparative analysis on different parameters like Power dissipation and Total propagation delay with respect to VDD and Temperature has been analyzed in 32nm, and 22nm and 16nm technology. . It was found that load less 4T SRAM cell consumes 45% less power as compared to 6T SRAM cell and occupies lesser area. All the simulations are been carried out on Tanner EDA Simulation tool.

**Keywords:** 6T Memory, 4T Memory, Load less, Power, Delay, Temperature.

## 1. INTRODUCTION

An SRAM (Static Random Access Memory) is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. The second driving force for SRAM technology is low power applications. Figure 1 shows a typical PC microprocessor memory configuration [2].

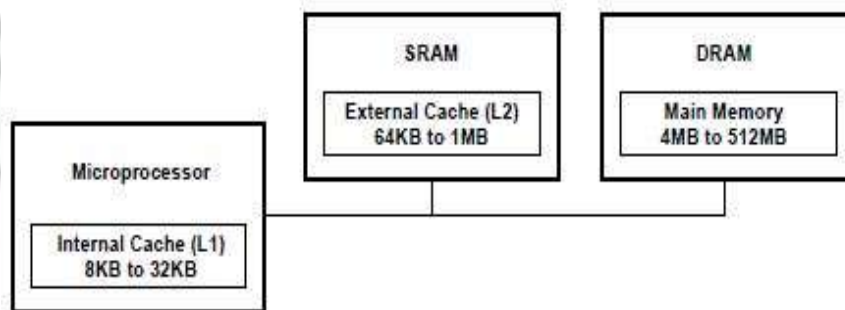


Figure 1 Typical PC Microprocessor Memory Configuration

## 2. LITERATURE REVIEW OF SRAM CELLS

### 2.1. 6T SRAM CELL

The schematic diagram of 6T SRAM cell is shown in figure 2. It consists of six transistors. Four transistors (M1–M4) comprise cross-coupled CMOS inverters and two NMOS transistors M5 and M6 provide read and write access to the cell. Upon the activation of the word line, the access transistors connect the two internal nodes of the cell to the true (BL) and the complementary (BLB) bit lines. [6]

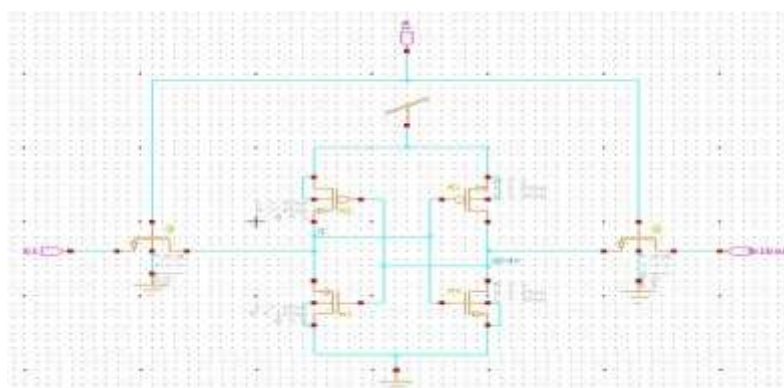
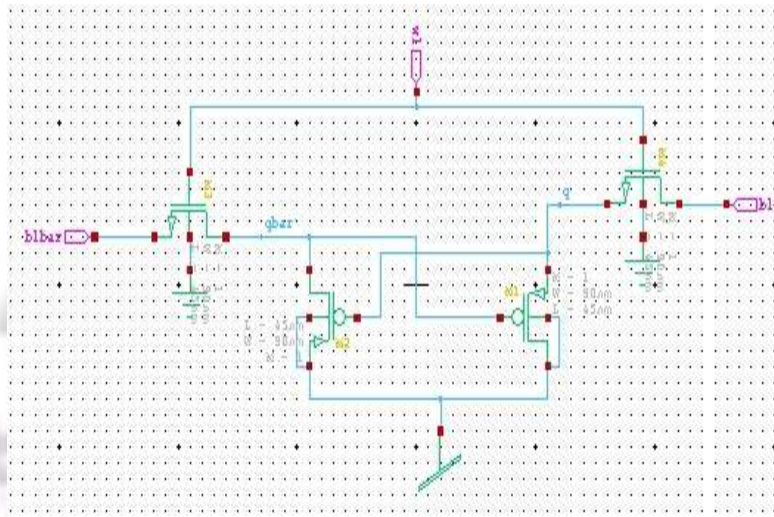


Figure 2 Schematic of 6T SRAM Cell

During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLBAR (bit line complement), depending on the stored data on nodes Q and QBAR. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD. [5]

## 2.2. 4T SRAM CELL

In the 4T-SRAM cell, two NMOS transistors are used as pass transistors to access the cell and two PMOS transistors are used as drivers for the cell. The bit lines are pre-charged to ground instead of VDD. For comparable speed and stability, the area occupancy and the power consumption of the load less 4T-SRAM cell is lesser than that of the conventional 6T-SRAM cell. The schematic diagram of 6T SRAM cell is shown in figure 3. [1]

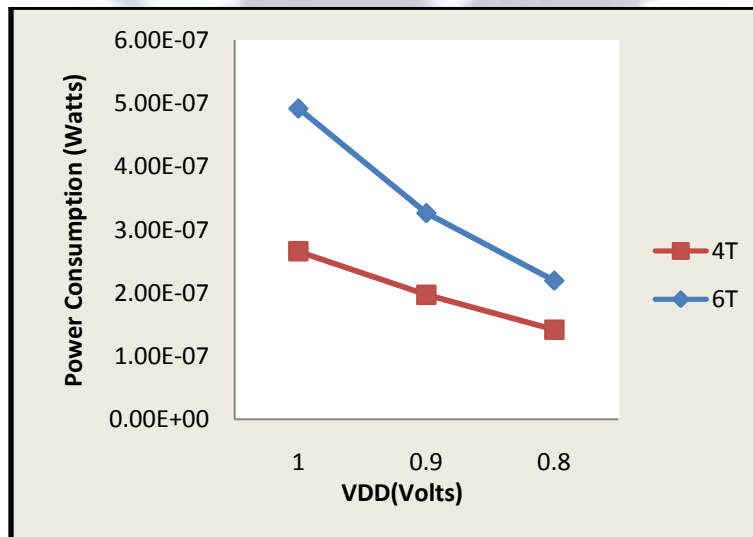


**Figure 3 Schematic of 4T SRAM Cell**

## 3. SIMULATION AND ANALYSIS

Both the circuits have been simulated in 32nm, 22nm and 16nm technology on Tanner EDA tool with supply voltage ranging. Figure 4-Figure15 shows comparative analysis of the circuits stated above.

### 3.1. AT 32nm TECHNOLOGY



**Figure 4 Power Consumption vs VDD for Different SRAM Cells**

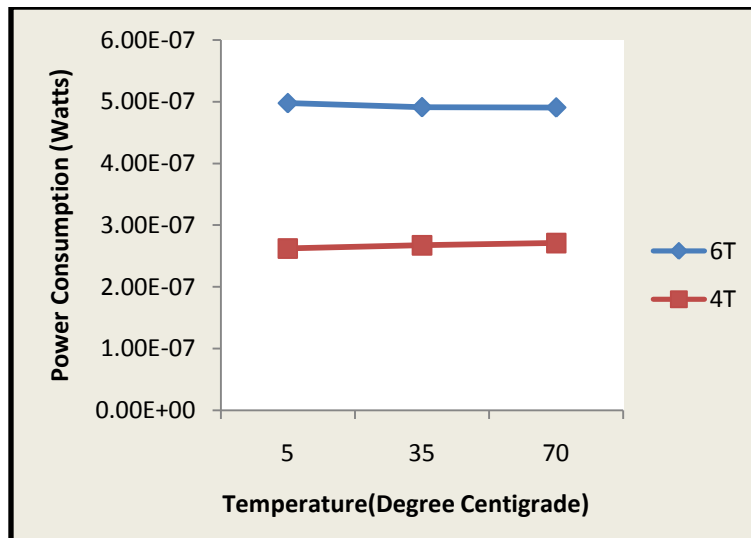


Figure 5 Power Consumption vs Operating Temperature for Different SRAM Cells (At VDD 1v)

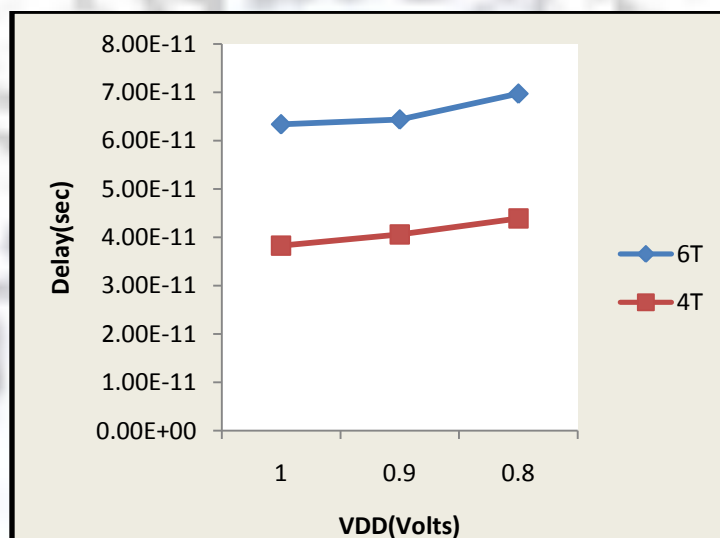


Figure 6 Delays vs. VDD for Different SRAM Cells

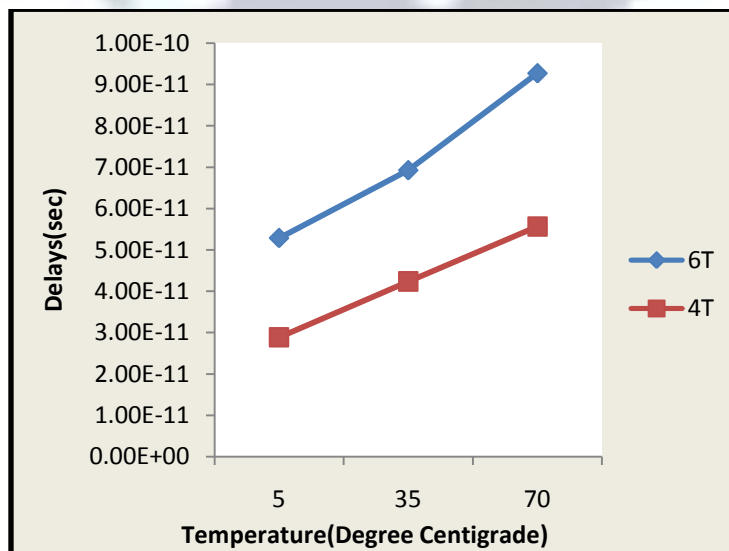


Figure 7 Delays vs Operating Temperature for Different SRAM Cells (At VDD 1v)

### 3.2. AT 22nm TECHNOLOGY

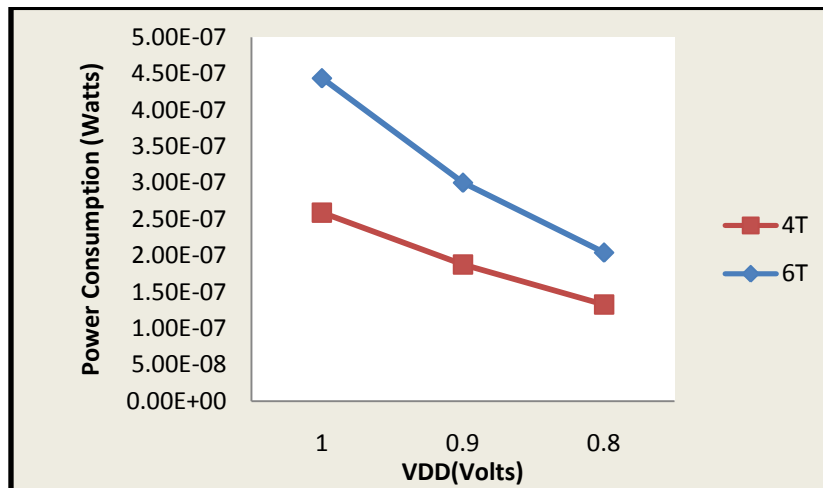


Figure 8 Power Consumption vs VDD for Different SRAM Cells

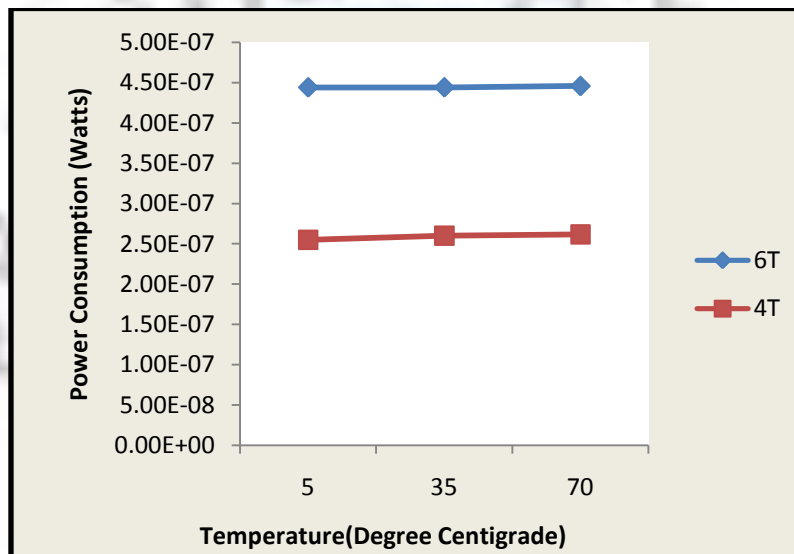


Figure 9 Power Consumption vs Operating Temperature for Different SRAM Cells (At VDD 1v)

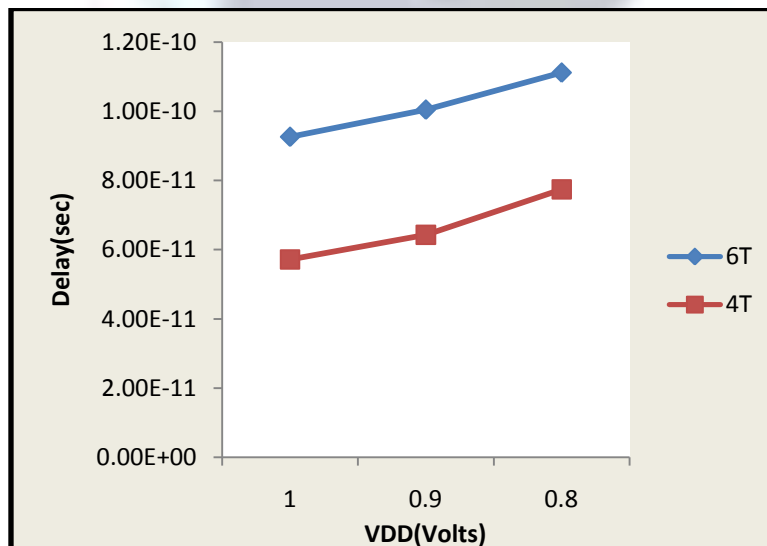


Figure 10 Delays vs. VDD for Different SRAM Cells

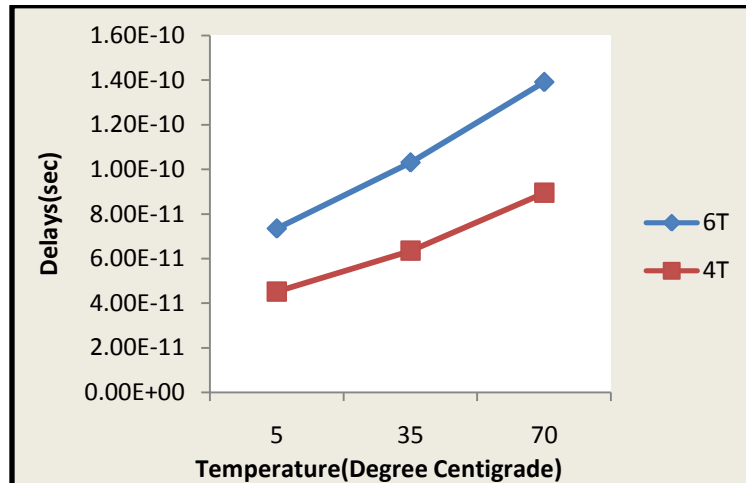


Figure 11 Delays vs Operating Temperature for Different SRAM Cells (At VDD 1v)

### 3.3. AT 16nm TECHNOLOGY

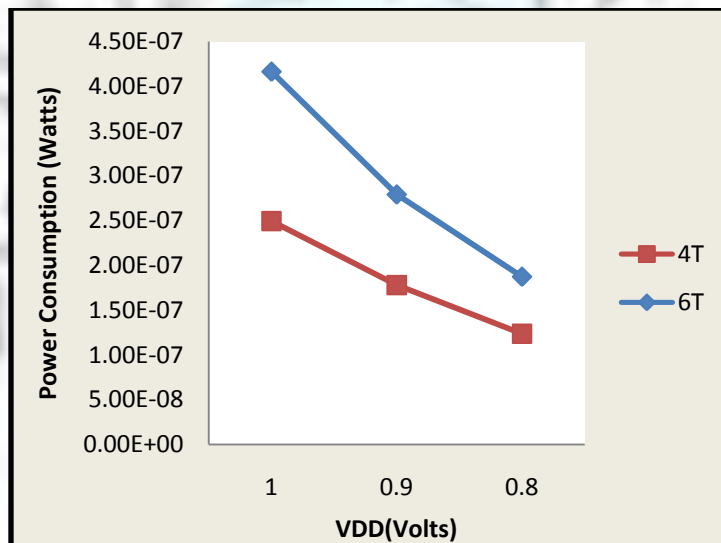


Figure 12 Power Consumption vs VDD for Different SRAM Cells

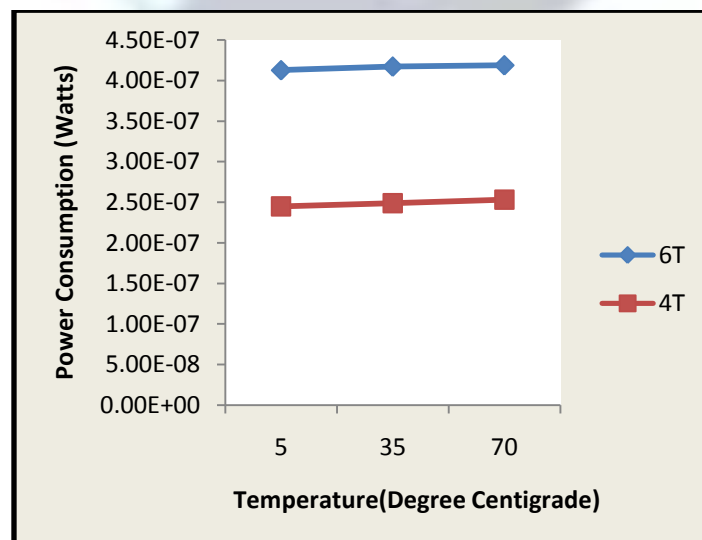


Figure 13 Power Consumption vs Operating Temperature for Different SRAM Cells (At VDD 1v)

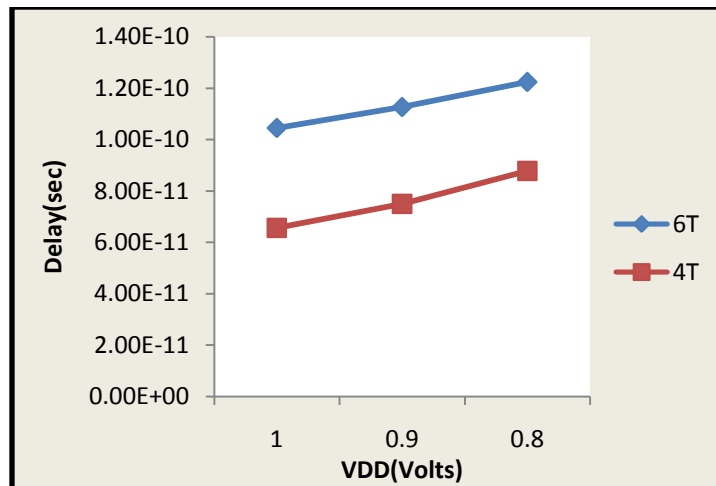


Figure 14 Delays vs. VDD for Different SRAM Cells

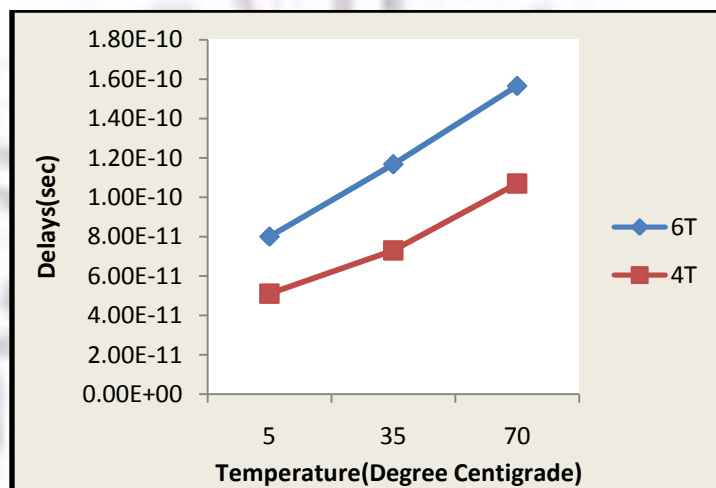


Figure 15 Delays vs Operating Temperature for Different SRAM Cells (At VDD 1v)

#### 4. OBSERVATIONS

The following are the observations of power delay product of different SRAM cells at different Technologies with supply voltage ranging.

Table 1 Power Delay Product comparison of different SRAM cells at 32 nm technology at 25C.

Different SRAM Cells	Power Delay Product(watts-seconds)		
	VDD=1v	VDD=0.9v	VDD=0.8v
6T	3.12E-17	2.10E-17	1.53E-17
4T	1.02E-17	8.00E-18	6.23E-18

Table 2 Power Delay Product comparison of different SRAM cells at 22 nm technology at 25C.

Different SRAM Cells	Power Delay Product(watts-seconds)		
	VDD=1v	VDD=0.9v	VDD=0.8v
6T	4.11E-17	3.02E-17	2.27E-17
4T	1.48E-17	1.21E-17	1.03E-17

**Table 3 Power Delay Product comparison of different SRAM cells at 16 nm technology at 25C.**

Different SRAM Cells	Power Delay Product(watts-seconds)		
	VDD=1v	VDD=0.9v	VDD=0.8v
6T	4.35E-17	3.14E-17	2.29E-17
4T	1.63E-17	1.33E-17	1.09E-17

### CONCLUSION

All the above figures depicts that 4T SRAM cell at 32nm, 22nm and 16nm technology shows better performance for the range of Power, delays and temperature than conventional 6T SRAM cell. It was found that load less 4T SRAM cell consumes 45% less power as compared to 6T SRAM cell and occupies lesser area. This paper tries to find out an efficient SRAM memory cell in both the aspects power consumption and speed in terms of power delay product at different technologies.

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