International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463
Vol. 3 Issue 11, November-2014, pp: (57-63), Impact Factor: 1.252, Available online at: www.erpublications.com

Simulation of Three, Five, Seven, Nine, Eleven, Thirteen and Fifteen Level Neutral Point Clamped Multilevel Inverter

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Abstract: Multilevel inverters (MLI) becomes more accepted over the last few years in high power application of electrical engineering with the advantage of less disturbances and the possibility to work at lower switching frequencies as compared to conventional two-level inverters. In this paper the simulation of single phase multilevel inverter is present. Simulation of three level, five level, seven level, nine level, eleven level, thirteen level and fifteen level inverters are done in MATLAB. These different level inverters are realized by neutral point clamped (NPC) or diode clamped topology of multilevel inverter. In this paper pulse width modulation control strategy is used for control the switches at appropriate conducting angles. The comparative results are presented for multilevel inverter up-to fifteen level which shows the total harmonic distortion is reduces as the number of level increases.

I INTRODUCTION

Multilevel converters (or inverters) have been used for dc-to-ac power conversion in high power applications such as utility and large motor drive applications. Multilevel inverters provide more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. There are three major multilevel topologies: cascaded, diode-clamped, and capacitor-clamped [l-11]. For the number of levels (M) or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. Instead, each voltage level can be supported by a capacitor and proper control [6-7, 1]. However, for M>3 and applications involved in active power transfer, such as motor drives, these multilevel converters all require either isolated dc power sources or a complicated voltage balancing circuit and control to support and maintain each voltage level [7]. In this aspect, the three existing multilevel converters are neither operable nor complete for real (active) power conversion because they all depend on outside circuits for voltage balancing. For the number of levels (M) no greater than 3 (i.e., M13), or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. The purpose of this paper is to increase the voltage level to achieve sinusoidal waveform & compare different voltage level by increasing the level through simulation. Various topologies of multilevel inverter have been investigated in the literature.

1.1 Flying capacitor multilevel inverter (FCMLI):

Many capacitors are required which makes this topology heavy and cumbersome. In this, load cannot be directly connected to generate the zero voltage level. Instead, the zero level is obtained by connecting the load to the positive or negative bar through the flying capacitor with opposite polarity with respect to the dc-link. [4]

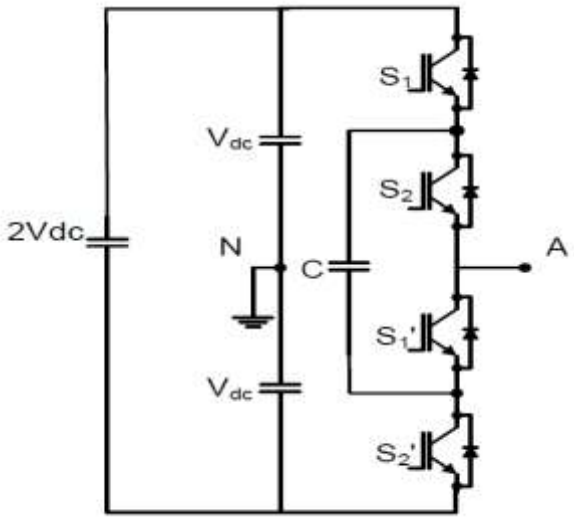

Figure 1.1: 3-level flying capacitor inverter [4]

1.2 Diode-clamped multilevel inverter:

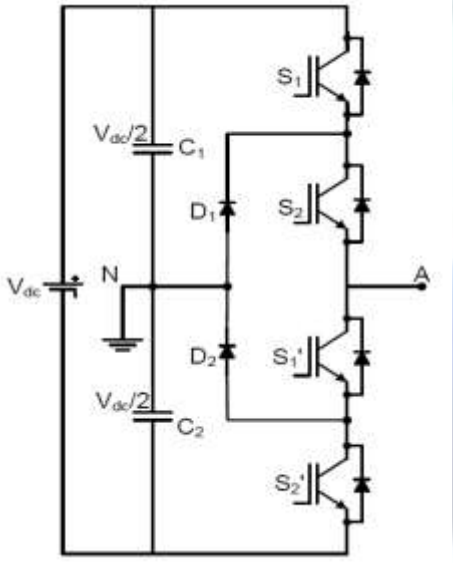

Figure 1.2: 3-level Diode-clamped inverter [4]

Diode-clamped multilevel inverter is the name given based on neutral-point clamped PWM inverter proposed to higher number of levels. The diode-clamped multilevel inverter has been wide accepted for its capability for high voltage with high efficiency in a efficient operation. An NPC-MLI inverter is mainly composed of two traditional two-level VSIs connected one over the other with the required modifications.

Here the name diode clamped (DC) makes more sense, since there are more voltage-level clamping nodes than only connected to the neutral N. As far as the main concern is the number of clamping diodes needed to share the voltage which is increased dramatically. This fact, together making difficulty to control the unbalancing problem the dc-link capacitor [6]. It is the most commonly used topology in the industry for a number of levels equal to three. An NPC-MLI inverter is mainly composed of two traditional two-level VSIs connected one over the other with the required modifications [4].

1.3 Cascaded H-Bridge multilevel inverter PWM H-bridge:

CHB-MLIs can be formed by the back to back series connection of two or more single-phase H-bridge inverters, hence as the name suggest cascade [11]. Each cascade H-bridge corresponds to voltage source in each bridge,. Therefore, a single H-

bridge converter is able to generate three different voltage levels. And series connection of N such bridges will be able to produce 2N+1 levels in the output of the inverter. This series connection is known as cascaded H-bridge multilevel inverter [4].

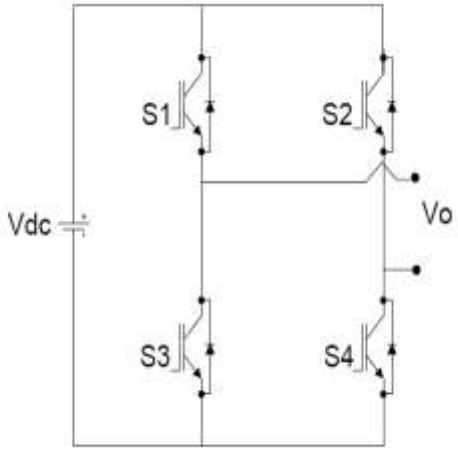

Figure 1.3: 3-level cascaded H-bridge inverter [4]

The multilevel inverters perform power conversion in multi- level voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability Considering these advantages multilevel inverters have been gaining considerable popularity in recent years. Comparing with two level inverter system having the same power, multilevel inverters has the advantages that the lower harmonic components on the output voltages, Electro Magnetic Interference (EMI) problem could be de- creased much. Due to these merits, many studies about multilevel inverters have been performed at simulation level [5].

Table 1: Comparison of conventional two level inverters and multilevel inverters [5].

S. No	Conventional inverter	Multilevel inverter
1	Higher THD in output voltage	Low THD in output voltage
2	More switching stresses on devices	Reduced switching stresses on devices
3	Not applicable for high voltage applications	Applicable for high voltage applications
4	Higher voltage levels are not produced	Higher voltage levels are produced
5	Since dv/dt is high, the EMI from system is high	Since dv/dt is low, the EMI from system is low
6	Higher switching frequency is used hence switching losses is high	Lower switching frequency can be used and hence reduction in switching losses
7	Power bus structure, control schemes are simple	Control scheme becomes complex as number of levels increases
8	Reliability is high	Reliability can be improved, rack swapping of levels is possible

II SIMULATION MODEL

Simulation is done in MATLAB to obtain the operation of multilevel inverter up-to fifteen level. Figure 2.1 shows the model which is developed in MATLAB for three level inverter. Subsystem shown in figure 2.1 represent the control strategy for switches.

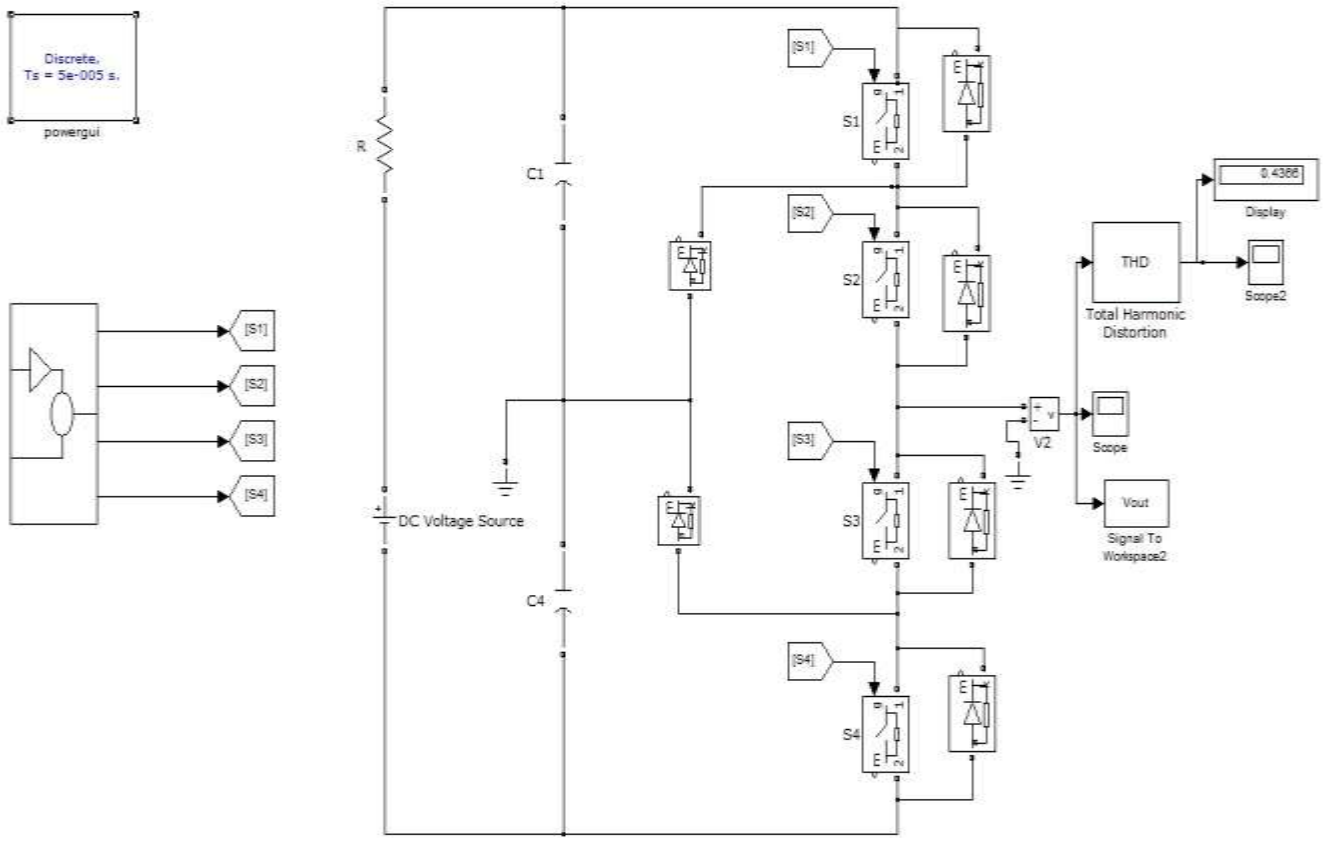

Figure 2.1: Simulation model in MATLAB of three level neutral point clamped inverter

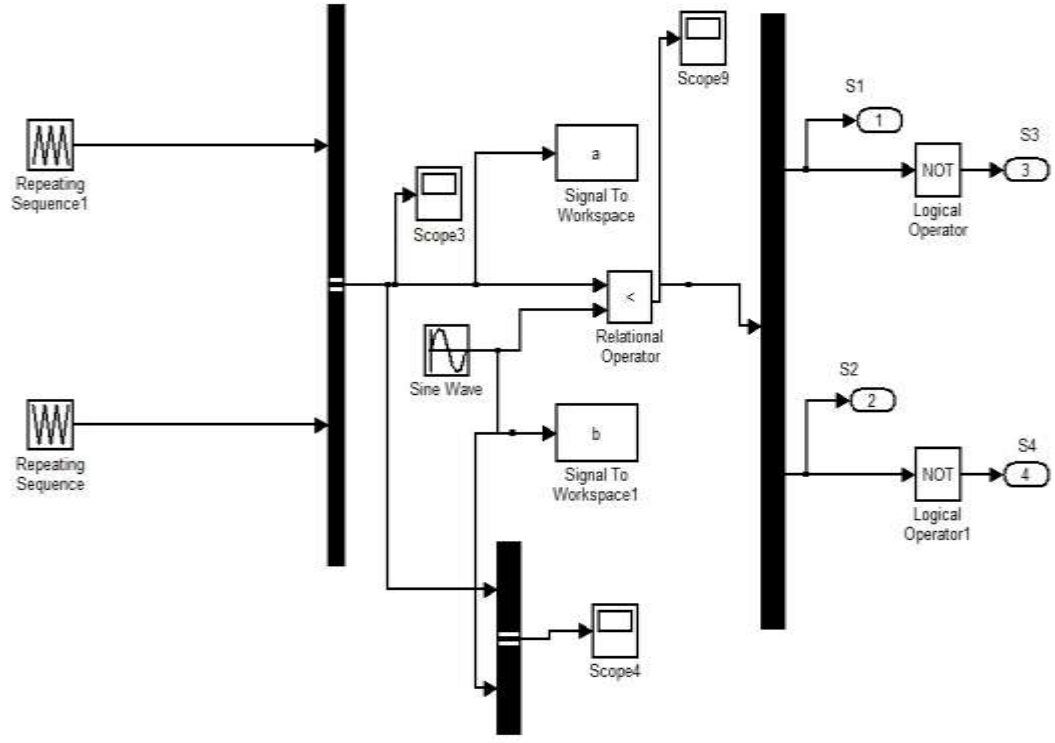

Figure 2.2: Subsystem for generating control signal for switching

For switching of the ideal diode sine pulse width modulation (SPWM) is used for modulation purpose Phase opposition disposition (POD) carrier scheme is used shown in figure 2.3.

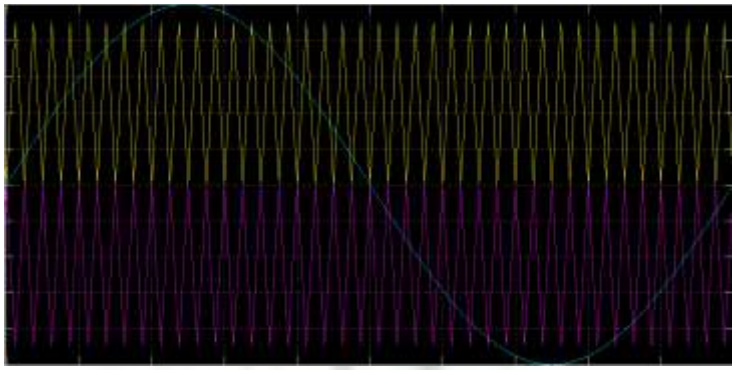

Fig 2.3: Sine Pulse width modulation for three level inverter

III RESULT AND DISCUSSION

Simulation results for three level, five level, seven level, nine level, eleven level, thirteen level and fifteen level inverter are shown in Figure 2.10, Figure 2.9, Figure 2.8, Figure 2.7, Figure 2.6, Figure 2.5 and Figure 2.4 respectively. And the total harmonic distortion for each inverter is shown in Table 3.1.

Table 3.1: thd of Three, Five, Seven, Nine, Eleven, Thirteen and Fifteen Level Inverters

Multilevel Inverter	Three Level Inverter	Five Level Inverter	Seven Level Inverter	Nine Level Inverter	Eleven Level Inverter	Thirteen Level Inverter	Fifteen Level Inverter
THD for voltage	43%	22%	15%	11%	8%	7.5%	7%

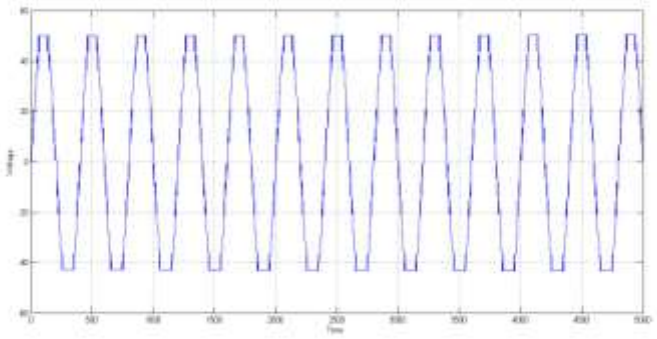

Fig 2.4 Simulation result of fifteen level Neutral point Clamped Multi Level Inverter

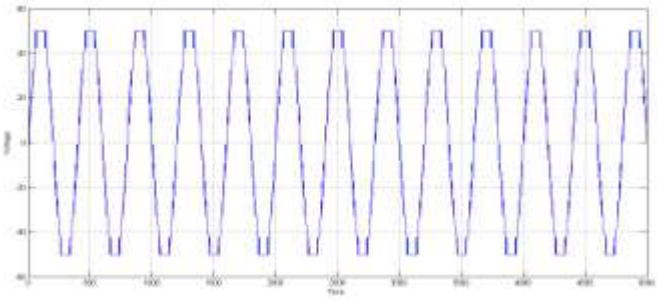

Fig 2.5 Simulation result of thirteen level Neutral point Clamped Multi Level Inverter

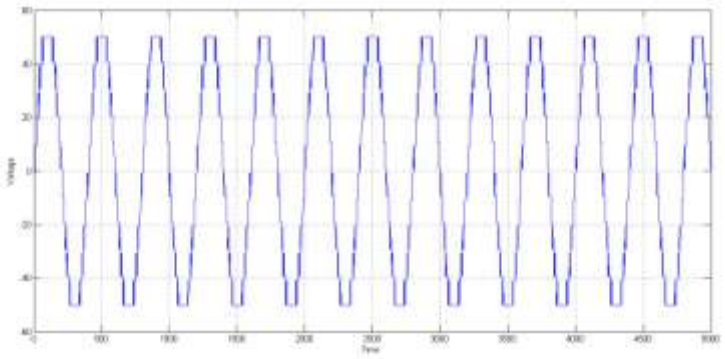

Fig 2.6 Simulation result of eleven level Neutral point Clamped Multi Level Inverter

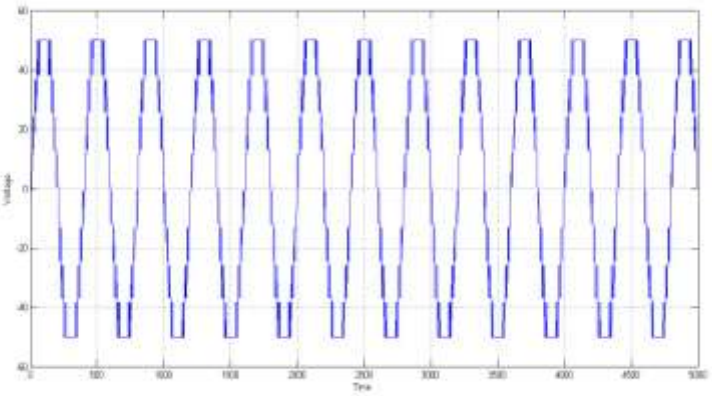

Fig 2.7 Simulation result of nine level Neutral point Clamped Multi Level Inverter

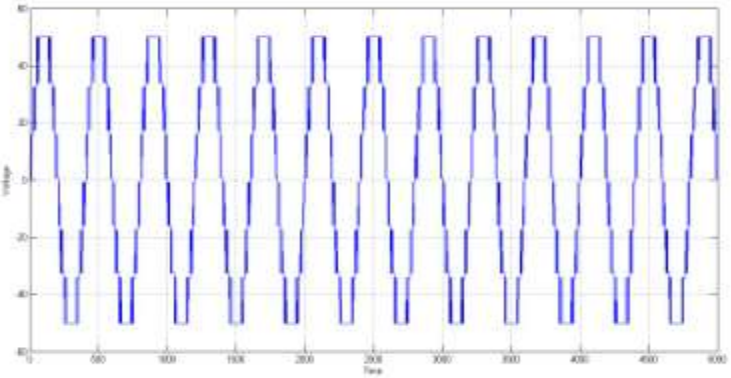

Fig 2.8 Simulation result of seven level Neutral point Clamped Multi Level Inverter

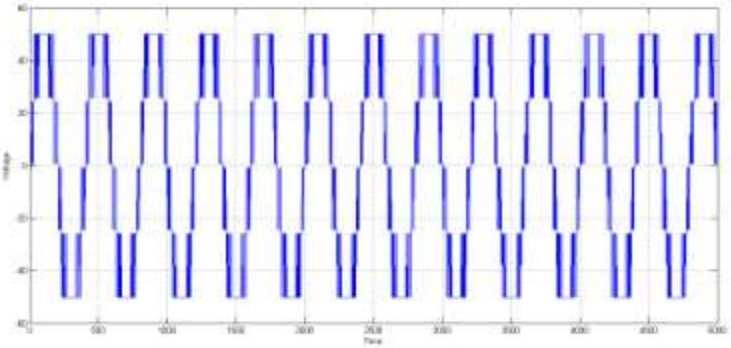

Fig 2.9 Simulation result of five level Neutral point Clamped Multi Level Inverter

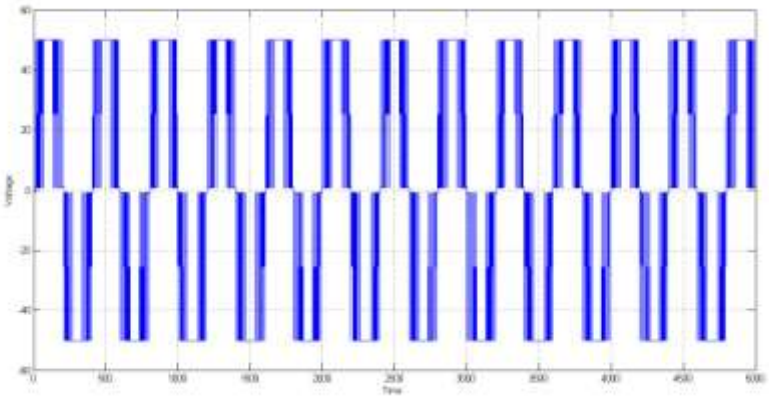

Fig 2.10 Simulation result of three level Neutral point Clamped Multi Level Inverter

CONCLUSION

The simulation of three level, five level, seven level, nine level, eleven level thirteen level and fifteen level inverters are realized in MATLAB SIMILINK where for switching of the ideal diode sine pulse width modulation (SPWM) is used for modulation purpose Phase opposition disposition (POD) carrier scheme is used. The total harmonic distortion for each level is calculated and compared. From the different levels of simulation it is clear that THD can be decreased by increasing number of levels.

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