International Journal of Enhanced Research in Management & Computer Applications
ISSN: 2319-7471, Vol. 6 Issue 7, July-2017, Impact Factor: 3.578

Design and Evaluation of Low Power Successive Approximation ADC

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ABSTRACT

Analog-to-digital converters (ADC) targeted for use in medical implant devices serve an important role as the interface between analog signal and digital processing system. Usually, low power consumption is required for a long battery lifetime. In such application which requires low power consumption and moderate speed and resolution, one of the most prevalently used ADC architectures is the successive approximation register (SAR) ADC. This paper presents a design of an ultra-low power 9-bit SAR ADC in 0.13µm CMOS technology. Based on a literature review of SAR ADC design, the proposed SAR ADC combines a capacitive DAC with S/H circuit, uses a binary-weighted capacitor array for the DAC and utilizes a dynamic latch comparator. Evaluation results show that at a supply voltage of 1.2V and an output rate of 1kS/s, the SAR ADC performs a total power consumption of 103nW and a signal-to-noise-and-distortion ratio of 54.4dB. Proper performance is achieved up to a supply voltage of 0.45V, with a power consumption of 16nW.

Keywords: Analog-to-digital converter (ADC), charge redistribution, CMOS, low power, low supply voltage, successive approximation, latched comparator.

I. INTRODUCTION

As signal processing is widely used in different fields, such as audio, control, communication and medical systems, the problem of dealing with both analog signal and digital signal becomes prevalent. Data converters serve such a role as the interface between the analog and digital world.

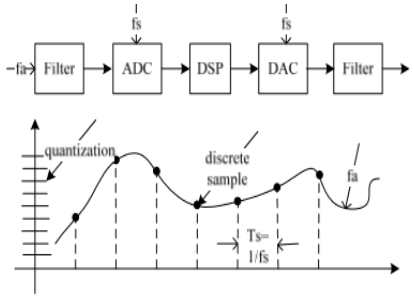


Fig. 1 Basic signal processing system [4]

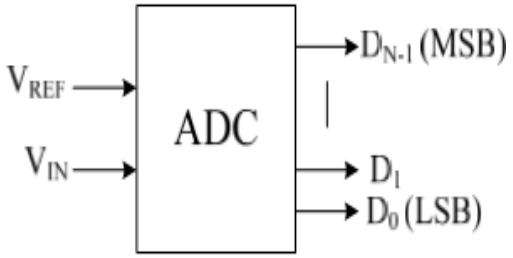


Fig. 2 Simplified block diagram of an ADC

Figure 1 describes a basic signal processing system. The analog input signal is first filtered to remove high-frequency components in order to avoid aliasing. Then the signal is sampled at frequency f_S and the discrete sampled data is digitized in the analog-to-digital converter (ADC). The digital outputs from ADC are executed in the digital signal processor (DSP). Finally, they return to an analog signal by the conversion of digital-to-analog converter (DAC) and removal of unevenness by the followed reconstruction filter.

This paper focuses on the canonic principles of ADC. Some normally used considerations of ADC such as resolution, aliasing and quantization error are described. ADC specifications regarding static and dynamic performance metrics are proposed. An overview of different ADC architectures is also described. Finally, comparison among the familiar architectures is described in terms of speed, power and resolution.

II. BASIC CONSIDERATIONS

Resolution: The resolution of an ADC is the number of its output words, which shows the minimum input voltage that an ADC can produce a code transition. Figure 2 shows a block diagram of an ADC. The smallest step is explained as the least-significant-bit (LSB) by equation $V_{LSB} = V_{REF}/2^N$, where V_{REF} is the reference voltage of the converter. The N-bit binary codes $D_0D_1\ldots D_{N-1}$ denotes the input voltage with a value of $(D_02^{-N}+D_12^{-N+1}+\ldots+D_{N-1}2^{-1})*V_{REF}$

Aliasing: When a discontinuous analog signal is sampled, it becomes a discreet signal. The sampling frequency should be at least two times greater than the signal frequency; otherwise, aliasing will be take place. This rule is known as Nyquist Criterion. It may cause in another different frequency and keep it hard to recover from the original one.

The phenomenon of aliasing can also be examined in the frequency domain (Figure 3). The analog signal has a band-limited spectrum F_X. If spectrum is sampled by a frequency Fs, the original spectrum will be replicated at frequencies multiplied with Fs. If the signal is under-sampled, which means Fs < 2Fx, the spectrums will converge and ruin the original signal spectrum. Thus the analog signal can barely recover.

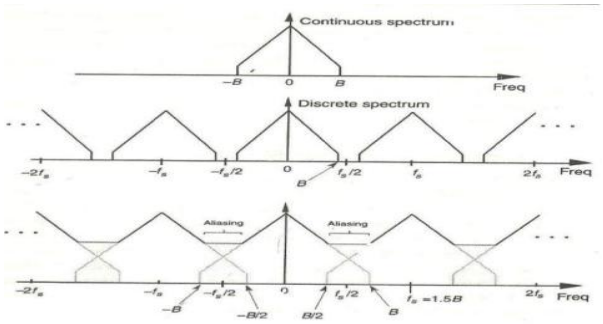
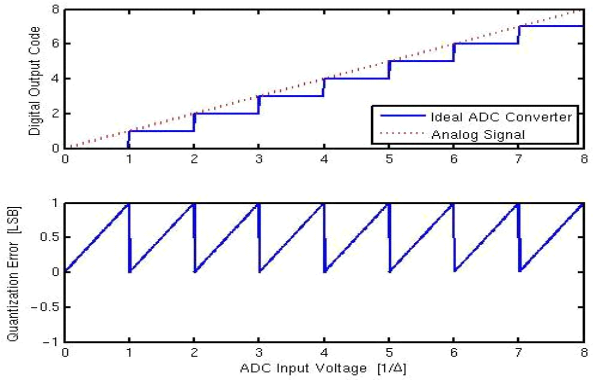


Fig. 3 Explanation of aliasing in frequency domain **Fig. 4 Probability density function of quantization error [5]**

There are two methods to figure out the problem of aliasing. First is to use a greater sampling frequency; the other is to use an additional anti-aliasing filter before sampling.

Quantization Error: ADC changes the analog signal to certain extents. The infinite analog information is converted to limited digital codes. During the quantization, even ideal ADC generates error, known as quantization error. Figure 4 demonstrates the analog signal and the digital output of a 3-bit ideal ADC. At the initiation of each code transition, there is no error. As the analog signal enhances, the error also becomes greater. The maximum error here is 1LSB (Δ).



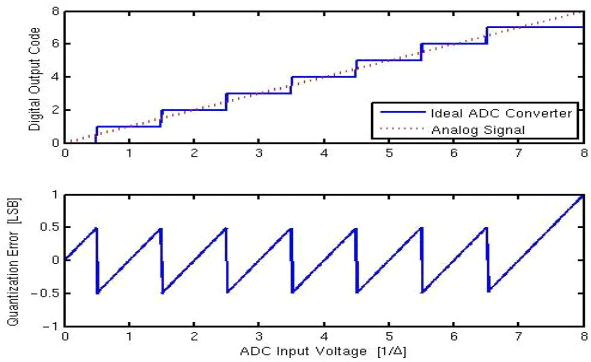


Fig. 4 Transfer characteristics and quantization error **Fig. 6 Shifted transfer characteristics and quantization error**

In order to make the quantization error be centralized about 0 and with a maximum error of ±1/2LSB, the above transfer curve is displaced to left by 1/2LSB.

The probability density function of the quantization error can be shaped as a uniformly distribution described in Figure 6 [5].

III. ADC PERFORMANCE METRICS

Static Performance: Static errors are divergence of conversion transfer characteristics from ideal one. The static performance of an ADC is described by these metrics: offset error, full-scale error, differential nonlinearity, integral nonlinearity and missing code.

a) Offset Error and Full-Scale Error*:* Offset error is the difference between the Ist code transition point and the ideal one; Full-scale error is the difference between the last code transition point and the ideal one.

b) Differential Nonlinearity (DNL): Differential nonlinearity is the difference between the ideal code width of 1LSB and the actual code width.

***c) Integral Nonlinearity (INL*)**: Integral nonlinearity is the difference between the actual code transition point and that of the ideal code transition. Moreover, INL is found equal to the accumulative sum of DNL [5].

d) Missing Codes: when the analog input enhances from zero to the full-scale value, not all the digital output codes are produced. This is known as missing codes.

Dynamic Performance: Static error is examined by DC signal, and it does not involve any information about noise and high frequency results. Opposite to static error, dynamic error is examined with periodic waveform, which gets extra information of ADC performance, such as SNR, SINAD, SFDR and ENOB

a)Signal-to-Noise Ratio (SNR)*:* For an ideal ADC, signal-to-noise ratio (SNR) is the ratio of an RMS (root mean square) full-scale input to its RMS quantization error [11].

$$V_{IN(\max)} = \frac{V_{ref}}{2\sqrt{2}} = \frac{2^N (LSB)}{2\sqrt{2}}$$

so

$$SNR = 20\log\frac{V_{IN(\max)}}{V_{error}} = 20\log\frac{2^N (LSB)/2\sqrt{2}}{LSB/\sqrt{12}} = 6.02N + 1.76$$

b) Signal-to-Noise-and-Distortion Ratio (SINAD)*:* Signal-to-noise-and-distortion ratio (SINAD) denotes the value of the input signal amplitude over the rms sum of all rest spectral components.

$$SINAD = 20\log_{10}(A_{SIGNAL}/(A_{NOISE} + A_{HD}))$$

c) Spurious-Free Dynamic Range*:* A Spurious-free dynamic range (SFDR) is the value of the input signal to the greatest spur, which is generally a harmonic of the input tone.

d) Effective Number of Bits*:* Effective number of bits (ENOB) is often used in place of the SINAD. It is often used to indicate ADC accuracy at a specific input frequency and sampling rate [11].

$$ENOB = \frac{SINAD(dB) - 1.76dB}{6.02dB/bit}$$

IV. PERFORMANCE EVALUATIONS

Testing environments to check the static and dynamic performance are set up. Conversion time of the ADC is simulated. Though speed is not a major concern in this work, by knowing the conversion time it is convenient for us to measure the design margin in terms of power and speed. Besides the power consumption simulated under the typical supply voltage (1.2V), it is also measured under some other low supply voltages (down to 0.4V) to investigate the minimum power figure.

Simulation Setup

The designed simulation setup is depicted in Figure 6 Input voltage, power supply, and reference voltage are all given as ideal source. A clock buffer is added between the ideal clock and the internal clock for the sake of driving the large capacitive load if necessary. A File write model written in verilog-A is used to save the ADC output data, which include 9-bit digital outputs, the input signal and the comparator output. All the above blocks are simulated in transistor-level by Cadence. The recorded data from Cadence is executed in MATLAB for calculating the static performance (DNL/INL/Offset) and the dynamic ones (SINAD/SFDR/ENOB).

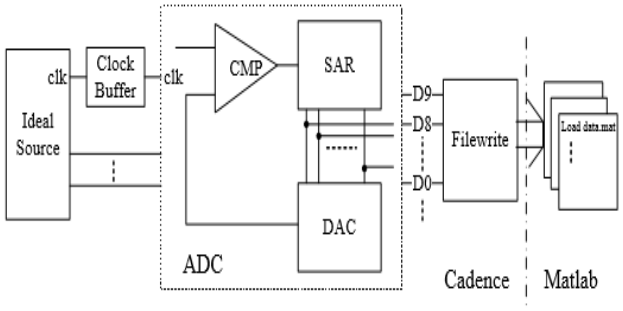


Fig. 7 Simulation Setup

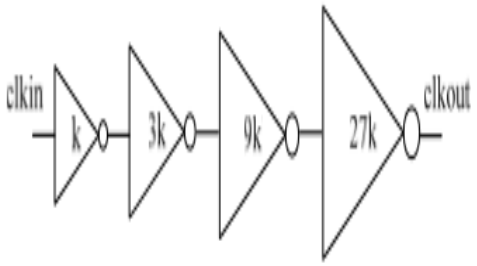


Fig. 8 Clock buffer contains a chain of 4 inverters

Clock Buffer: The clock synchronizes all the data transfer on the chip. The number of total clock load could be very large. In order to get an on-chip clock with relatively sharp rise and fall edge, clock buffer is critical to drive such a big load. Figure 7 shows the block diagram of the clock buffer.

Ideal Sources: The typical supply voltage is 1.2V according to 0.13μm CMOS process. The reference voltage for the ADC is chosen as 0.8V. The analog input has a range from 0 to V_{REF}. If V_{REF} is set as the same value of V_{DD}, the comparator won't work correctly due to the extra large input voltage. Therefore, V_{REF} is chosen a value as $2/3*V_{DD}$.

$$V_{COMP} = -V_{IN} + D_8\frac{V_{REF}}{2} + D_7\frac{V_{REF}}{4} + \cdots + D_1\frac{V_{REF}}{2^8} + D_0\frac{V_{REF}}{2^9} + V_{REF}$$

V_{COMP} and blue lines are used for V_{REF}. The waveforms match our expectations and the ADC gets a digital output of 101010100_2, the same as the value by calculation.

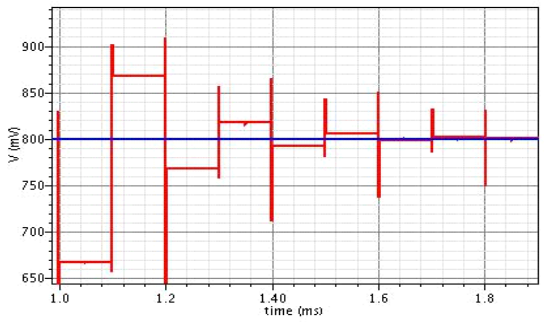


Fig. 9 Simulation plots of V_{COMP} and V_{REF}

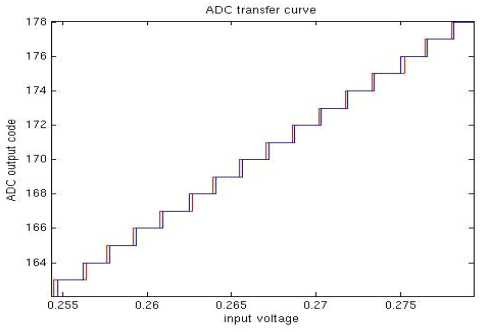


Fig. 10 ADC transfer curve, ideal and simulation

Figure 10 shows part of the input/output transfer curve. The blue line stands for the simulation result, and the red line is an ideal transfer curve. Based on these two lines, non-linearity error and offset error are calculated.

Figure 11 shows the DNL and INL plots respectively. From the figure, it can be seen that the maximum DNL is +0.26/-0.25 LSB, and the maximum INL is +0.31/-0.23 LSB.

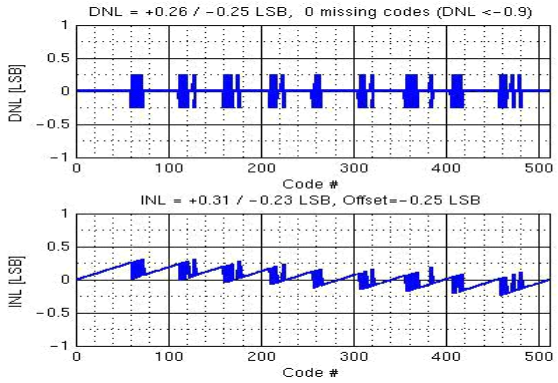


Figure 11 Matlab results of static error measurements

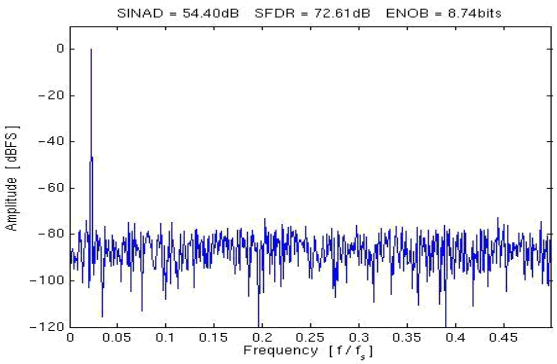


Figure 12 Measured FFT spectrum at 22.46Hz input signal frequency

Mathematically, refer to [3], this can be expressed as:

$$f = \frac{M_C}{M} f_s \qquad [3]$$

Where
f is the signal frequency
f_s is the sampling frequency
M_C is the number of cycles per record
M is the record length

In our measurement, we use the sampling frequency f_s with a value of 1KHz. A length of 1024 samples is recorded from 23 sine cycles. Based on the above equation, we get the signal frequency as a value of 22.4609372Hz. Figure 11 shows the spectrum of the digital data after Fourier transform. The resulting SINAD is 54.4dB and the SFDR is 72.6 dB. Based on SINAD, we get the ENOB as 8.74 bits.

Conversion Time: The conversion time of the ADC depends on the following: the time for comparator to make a decision, the duration of sampling, the time for DAC to be settled down and the clock-to-q delay for DFF in SAR. The last item can almost be neglected compared to the first three ones. So the total conversion time is defined as:

TCONV = TSAMPLE_MSBB + 9 (TDAC_MSB + TCOMP)

Table I gives the simulation results. The total conversion time is 167ns, which is much faster than our specified sampling time (1ms).

Table I Speed simulation

Block	Delay	Unit
Comparator	1.3	ns
DAC_MSB	15	ns
Sample	20	ns
Total	166.7	ns

V. POWER CONSUMPTION

The total power consumption of a CMOS circuit can be expressed by three items: dynamic power consumption, leakage power consumption and direct-path consumption [5]. The dominant factor is the dynamic power based on the equation: CfV^2. The ADC is simulated with a sampling rate of 1kS/s. The analog input signal is set as a frequency of 500Hz. Command .AVG is used in SPICE to calculate the average power consumption. Table II shows both the total power and block power. In total, the ADC consumes an average power of 103nW, which is a quite small number. Figure 13 gives a pie chart which describes how the power is distributed. SAR consumes more than half of the total power, while the comparator which utilizes a dynamic latch only consumes 4% of the total power.

Table II Power consumption simulation

Block	Power	Unit
SAR	69.2	nW
DAC	21.7	nW
Comparator	4.2	nW
Clock buffer	7.8	nW
Power exclude clock buffer	95.1	nW
Total power	103	nW

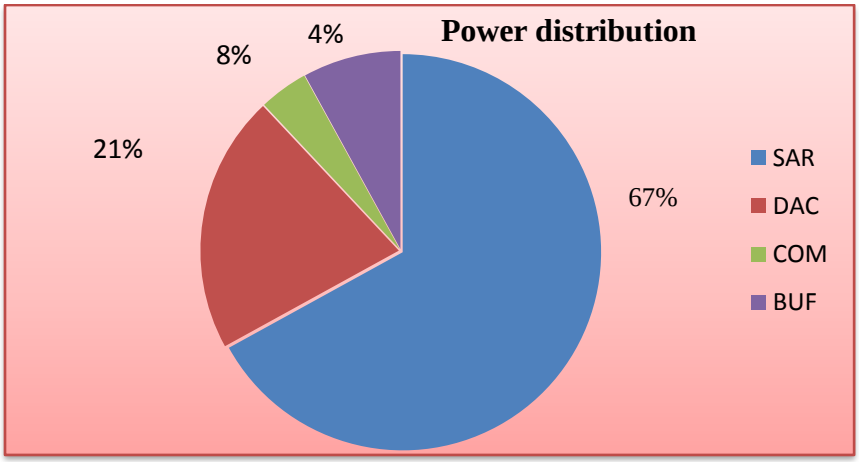


Fig. 13 Pie chart of power distribution

Low Supply Voltage Simulation

Based on the above simulations, we've completed the performance characterization of our ADC. A summarize is given in Table III.

Table III Performance summarize for ADC

Parameters	**Result**	**Unit**
Technology	ST0.13μm	-
Supply Voltage	1.2	V
Resolution	9	bits
Input Range	0 - 0.8	V
Sampling Frequency	1	kS/s
Power Consumption	103	nW
Conversion Time	167	ns
DNL	0.26/-0.25	LSB
INL	0.31/-0.23	LSB
Offset	-0.25	LSB
SINAD(f=22.46Hz@1kHz)	54.4	dB
SFDR(f=22.46Hz@1kHz)	72.7	dB
ENOB(f=22.46Hz@1kHz)	8.7	bits

As the supply voltage has a large effect on the dynamic power, it is interesting to investigate the power bound of the ADC by decreasing the supply voltage. Simulation data under various supply voltage are summarized in Table IV. Moreover, Figure 14 (a) and (b) shows power and SINAD as a function of supply voltage. A relatively high SINAD value is obtained down to a supply voltage of 0.45V, and the total power becomes 16nW, which saves 84% power compared to the original value 103nW.

Table IV ADC performance under different supply voltage

Supply Voltage[V]	1.2	0.9	0.6	0.45	0.4
Voltage Reference [V]	0.8	0.6	0.4	0.3	0.25
Input Range [V]	0.8	0.6	0.4	0.3	0.25
SINAD [dB]	54.4	54.2	53.8	53.6	49.3
ENOB [bit]	8.74	8.71	8.7	8.6	7.9
Power Consumption [nW]	104	54.3	26	16	13.2

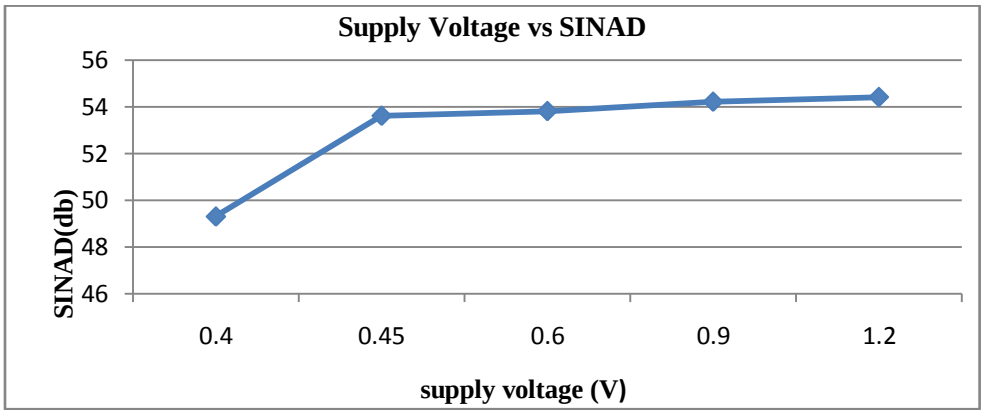


Fig. 14 (a)) Supply voltage versus SINAD

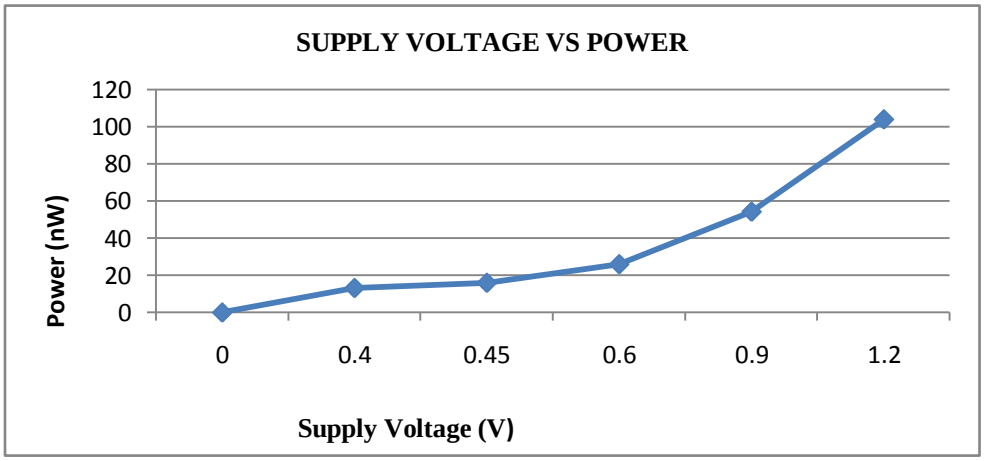


Fig. 14 (b) Supply voltage versus power

In this work, a 9-bit 1kS/s 1.2V SAR ADC is proposed in transistor level and it gains a very low power with good result. To minimize power, this ADC: 1) adds the capacitive DAC with S/H circuit; 2) uses the binary-weighted capacitor array for the DAC; 3) uses the dynamic latch comparator.

CONCLUSION

The comparator is often a critical part in a data conversion system. In this work, great attempts are done on the modeling of the comparator. Different topologies of comparator are analyzed and compared. A dynamic latch comparator is selected for its lowest power consumption. However, it produces more drawback noise which degrades the input resolution and degrades SNR. To get over this difficulty, isolation switches are added ahead the input stage of comparator, By this way keep the input signals away from the noise. Moreover, a latch is preceded after the comparator to keep the previous output unaltered in the whole clock cycle. Such operation avoids unnecessary charge and saves power.

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