International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463
Vol. 3 Issue 6, June-2014, pp: (473-476), Impact Factor: 1.252, Available online at: www.erpublications.com

CW Wideband Radar Receiver with Digital Noise Reduction Algorithm

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Abstract: Here we present a Continuous Wave radar receiver with a digital noise cancellation circuit. The leakage signal is cancelled by the mixer/PLL followed by an analog low pass filter also works as anti aliasing filter for the A-to-D. The digital signal processing after A-to-D cancels the analog thermal noise from front end which is mathematically AWGN in nature. We assume synchronous CDMA transmission. So, after noise cancellation by DFC algorithm we use a Data recovery Phase locked loop to lock onto phase of the reflected wave and get its magnitude. These data are used to find the range and location of the object.

Keywords: CW radar, PLL, A-to-D, DPLL, DFC and synchronous CDMA.

1.0 INTRODUCTION

A great deal of technological ground work is done for continuous wave radar since World War II. Continuous wave radar transmits electromagnetic wave continuously and receives the reflected wave from different objects. The signal processor calculates the magnitude and phase delay of the echo and calculate the location of the object. Subsequently, the radar is used for air traffic control, space surveillance and battlefield air defense system [1].

The signal processing associated with radar can be divided into analog and digital domain [2]. We have to cancel the leakage signal and magnify the echo at the same time. CMOS analog circuits are noisy, which limits the digital dynamic range after A-to-D. Recently there is a huge interest in analog noise cancellation circuit. But this paper presents a novel method of noise cancellation in digital, thus increasing the dynamic range. A digital delay estimator is also discussed here.

The section I introduce the subject and signify the motivation of this paper and in section II we introduce the radar receiver structure. The next section we discuss about the front end of the radar receiver. The section IV discusses about the method of noise reduction following an A-to-D. Also a PLL is used to find the chip and bit timing of the received data sequence. In section V, the amplitude and phase delay of the reflected wave are calculated. In the next section we conclude the paper.

2.0 CW Radar receiver

The signal that reaches the receiving antenna is given by:

$$r(t) = A(t)sin(wt) + a(t-\tau)\sin\big(w(t-\tau)\big) + Noise$$

where, *A(t)* is transmitted signal and *a(t-□)*is the reflected wave. Now we have to cancel or attenuate the first term and the third term. We first subtract the term which is the transmitted signal, from *r(t)* and get *r1(t).*

$$r_1(t) = A_1(t)sin(wt) + a(t-\tau)\sin\big(w(t-\tau)\big) + Noise$$

This term is passed through a low noise amplifier circuit, so we get the output signal:

$$r_2(t) = A_2(t)sin(wt) + a_2(t-\tau)\sin\big(w(t-\tau)\big) + Noise$$

Here the first term is cancelled by heterodyne mixer, where the quadrature phase is minimized to get the correct frequency and phase and we get the *cos(wt)* term to the in-phase super heterodyne mixer. The output of the low pass filter will be,

$$r_3(t) = a_3(t-\tau)\sin(w\tau) + Noise$$

The mixer is followed by an analog low pass filter, and a gain stage. The term will be digitized by an A-to-D, where a noise reduction circuit is used to reduce the noise. This noise reduction circuit is implemented by a method called Decision Feedback Cancellation Algorithm

3.0 Front End of the Receiver

The transmitted signal is subtracted from the received signal, but some leakage amount of voltage will remain. So we have to attenuate the first term further. But we amplify the signal by low noise amplifier.

Now we have choices to make: In-phase or in-phase and quadrature-phase, direct down conversion or super heterodyne structure of mixer. Our choice is In-phase component only in transmission and super heterodyne structure.

Here we take the signal In-phase signal which is

$$r(t) = A(t)sin(wt) + a(t-\tau)\sin\big(w(t-\tau)\big) + Noise$$

and we put a PLL to lock on the signal. The VCO output will be *sin(wt)* and we find the *cos(wt)* signal. The *cos(wt)* is used to mix the signal given below to cancel the $A_2(t)sin(wt)$ term.

$$r_2(t) = A_2(t)sin(wt) + a_2(t-\tau)\sin\big(w(t-\tau)\big) + Noise$$

We get after mixing

$$r_2(t)\cos(wt) = \frac{A_2(t)}{2}sin(2wt) + \frac{a_2(t-\tau)}{2}[\sin(2\text{wt})\cos(w\tau) + (\cos(2wt)+1)\sin(w\tau)] + Noise$$

After passing through low pass filter we get

$$r_3(t) = 0.5a_2(t-\tau)\sin(w\tau) + Noise$$

4.0 Digital Noise Reduction Algorithm

References [3][4][5] give a detail description of an algorithm, which is derived from Subtractive Interference Cancellation scheme used in Code Division Multiple Access. Here we use the algorithm to reduce the noise which is Additive White Gaussian Noise (AWGN). The A-to-D digitizes $r_3(t)$ and the $a_2(t-\tau)$ can be written as,

$$r_4(t) = \sum_{i=1}^{2L} a_i b_i C_i + Noise$$

We assume that $r_4(t)$ is the input to the DFC and the output estimate will be,

$$\hat{b}_1 = 2\sum_{i=1}^{2L} a_i b_i C_i C_1^t - \frac{1}{L^2}\sum_{k=1}^{2L}\sum_{i=1}^{2L} a_i b_i C_i C_k{}^t C_k C_1^t + \frac{2NC_1^t}{L} - \frac{1}{L}\sum_{k=1}^{2L} NC_k^t C_k C_1^t$$

Now first we consider a case where all $a_i=1$ and $b_i=1$; the signal will be equal to $1/L(1-1/L)$. The noise variance will be $4*(L-1)/2/L^4$ if the input noise power $\sigma^2=1$. So we get SNR of $1/L^2$.

Now using the estimate of the bit we form a clean signal which has low noise. We can use the clean signal to pass through DFC stages again to reduce the noise further.

5.0 The Phase delay estimation

We sample and hold the analog signal before digitizing and using the Noise cancellation algorithm which is DFC. We have to know the exact chip timing and bit timing otherwise the noise cancellation circuit will not work. We form he clean signal (pass it through DAC) and correlate with the analog signal and pass the signal to a VCO. Now the VCO output should be the clock twice of the chip rate. This is done by a Data recovery PLL. Now once the chip clock is there, we find the bit timing which is easy as the bits are all 'one' and it is shifted m-sequence.

The last part is phase delay estimation which is done by a computer. The transmitted signal is with the computer and we consider a long sequence like, (all'1', all'-1', and a long PRN sequence). This long sequence of data is correlated with the data sequence recovered from the reflected wave and the phase delay estimated. The amplitude will be average of the amplitudes found in the bits from the reflected wave. So we can find the range from the delay or the attenuation of the signal.

6.0 CONCLUSION

In this paper we present novel methods of signal attenuation which is unwanted and noise attenuation which is done in digital domain. The received CW wideband signal is down converted by super heterodyne structure. The transmitted signal is wideband in nature and actually is a synchronous CDMA signal. It can accurately find the range and from the differing range we can find the velocity of the object. If it is a big object like planets and stars we can plot the image of them.

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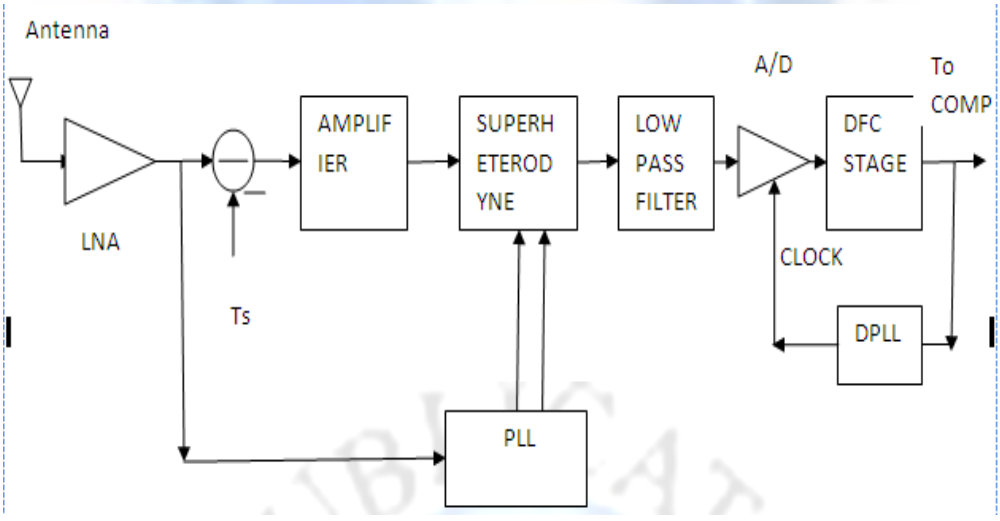

Figure 1: Block diagram of CW Radar Receiver. Ts is the transmitted signal

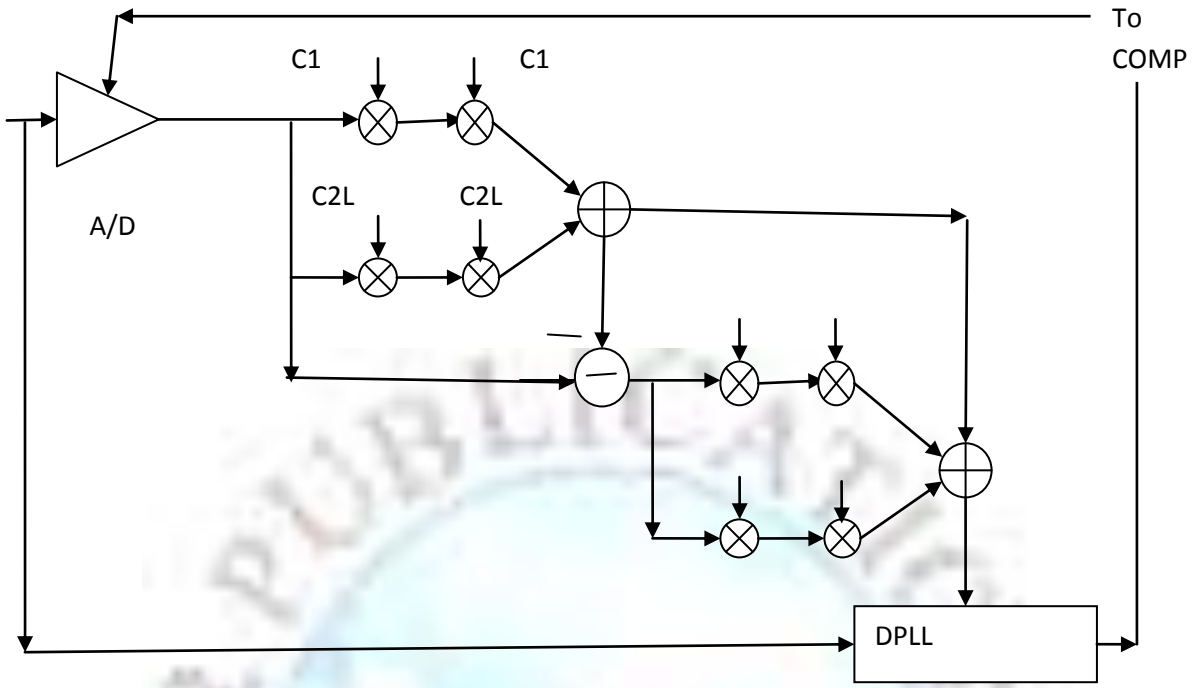

Figure 2: Noise Cancelling DFC Structure and A/D sampling clock recovery by DPLL