International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463
Vol. 3 Issue 6, June-2014, pp: (484-490), Impact Factor: 1.252, Available online at: www.erpublications.com

Performance Analysis of Low Power 4T, 6T and 8T SRAM Cells at 32nm Technology

Sandeep Rehlan[1], Ashutosh Yadav[2], Poonam[3], Supriya Bhutani[4]

[14]Electronics Department, PPIMT, Haryana, India
[2]Electronics Department, MDU, Haryana, India
[3]Electronics Department, OITM, Haryana, India

Abstract: **The power consumption has become an important consideration on the VLSI system design and microprocessor as the demand for the portable devices and embedded systems continuously increases. Today's microprocessors are very fast and require fast caches with low power dissipation and low delay. The write power is usually larger than the read power due to large power dissipation in driving the cell bit lines to full swing. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represents the active power consumption. The power dissipated in bit-lines represents 70 per cent of the total SRAM power consumption during a write operation. Many techniques have been proposed to reduce the write power consumption by reducing the voltage swing level on the bit lines. In this paper, 4T, 6T and 8T SRAM cells are compared on the basis of power consumption and propagation delay with the variation in V_{dd}. The technology used to implement the 4T, 6T and 8T SRAM cell is 32nm CMOS technology and the software used is Tanner Tool. Schematic of the SRAM cell is designed on S-Edit and Net list Simulation done by using T-Spice and waveforms are analyzed through W-EDIT.**

Keywords: VLSI, Vdd, CMOS Logic, Low Power, 4T SRAM, 6T SRAM, 8T SRAM.

1. INTRODUCTION

An SRAM (Static Random Access Memory) is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. Figure 1.1 shows a typical PC microprocessor memory configuration.

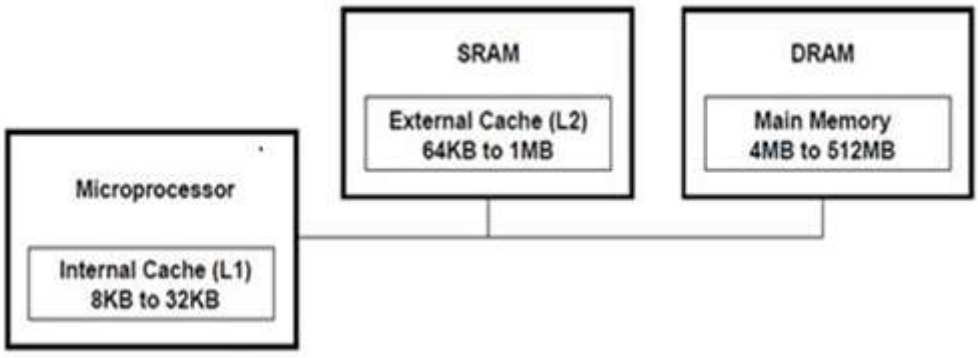

Figure 1: Typical PC Microprocessor Memory Configuration

Static random-access memory (SRAM) is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. The word static here points that it needs not to be refreshed periodically unlike dynamic random access memory. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. There are many reasons to use an SRAM or a DRAM in a system design. Design parameters include density, speed, volatility, cost, and features. All of these factors should be considered before you select a RAM for your system design. Our focus is to make the general use device like computer more compact in terms of size, better speed, less power consumption and so we are moving towards the new technology [3].

2. SRAM CELL DESIGN

2.1 4T SRAM Cell

The 4T SRAM Cell shown in Figure 1, the resistors are replaced with the two PMOS transistors. This cell shows greater stability and low power dissipation as compared to the cell in this section. PMOS being a semiconductor device, consume less power as compared to the resistors used in previous cell. The cell size is 35.45% smaller than a conventional 6T cell using same design rules. Read operation performed from one side and write operation performed from other side of cell. When '0' stored in cell, load and driver transistor are ON and there is feedback between ST node and STB node, therefore ST node pulled to GND by drive transistor and STB node pulled to V_{dd} by load transistor. And when '1' stored in cell, load and driver transistor are OFF and for data retention without refresh cycle following condition must be satisfied.

I_{off}-NMOS-access $\geq 3 \times$ (IDS-Load - IG-Driver)
I_{off}-PMOS-access $\geq 3 \times$ (IDS- Driver - IG- Load)

For satisfying above condition when '1' stored in cell, we use leakage current of access transistor, especially sub threshold current of access transistors. For this purpose during idle mode (when read and write operation don't performed on cell) of cell, BL and BLB maintained at V_{dd} and GND, respectively and word-line and wordline-2 maintained on VIdle1 and VIdle2, respectively. Most of leakage current of access transistors is sub threshold current since these transistors maintained in sub threshold condition. Simulation result in standard 45nm technology shows if during idle mode of cell, BL and BLB maintained at VDD and GND respectively, and VIdle1=0.5V and VIdle2=1.1V '1'stored in cell without refresh cycle and thus in idle mode [1].

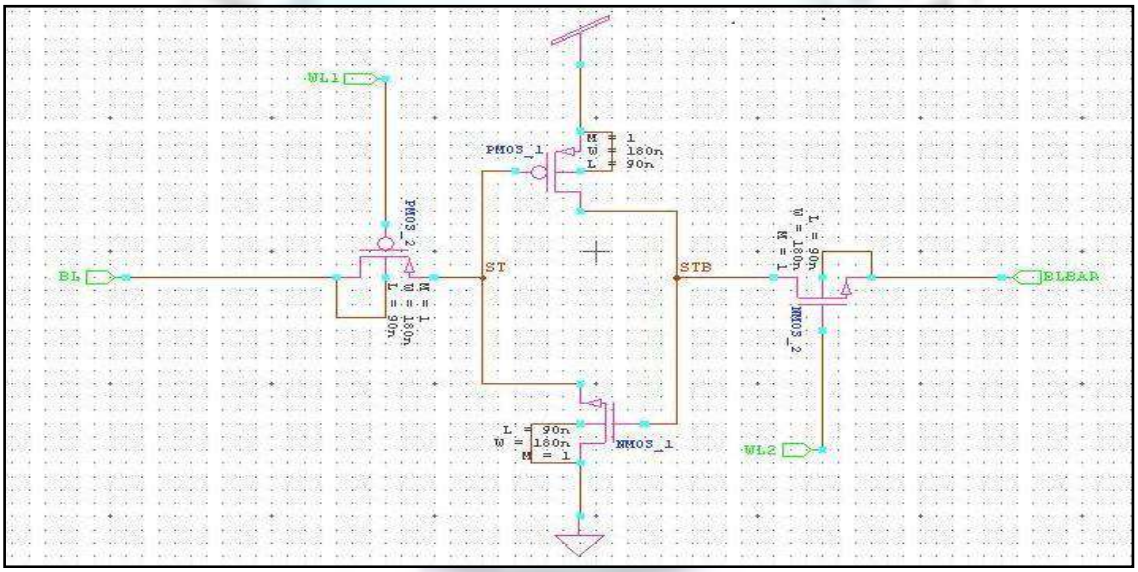

Figure 2: S-Edit Schematic of 4T SRAM Cell

2.2 Write Operation

When a write operation is issued the memory cell will go through the following steps.

Bit-line driving: For a write, complement of data placed on BLB, and then word-line1 asserted to V_{dd}, but voltages on word-line2 and BL maintained at idle mode (V word- line2=VIdle2 and VBL=V_{dd}).

Cell flipping: This step includes two states as follows.

(a) Complement of data is zero: in this state, STB node pulled down to GND by NMOS access transistor, and therefore the drive transistor will be OFF, and ST node will be floated and then pulled up to voltage of BL (V_{dd}) by leakage current (most of this current is sub-threshold current) of PMOS access transistor, and thus load transistor will be OFF.
(b) Complement of data is one: in this state, STB node pulled up to V_{dd}-Vtn by NMOS access transistor, and therefore the drive transistor will be ON , and ST node will be pulled down to GND, thus load transistor will be ON and STB node pulled up to V_{dd}.

Idle mode: At the end of write operation, cell will go to idle mode and word-line1 and BLB asserted to VIdle1 and GND respectively.

2.3 Read Operation

When a read operation is issued the memory cell will go through the following steps.

Bit-line Pre-charging: For a read, BL pre-charged to V_{dd}, and then floated. Since, in idle mode BL maintained at V_{dd}, this step didn't include any dynamic energy consumption.

Word-line activation: in this step word-line2 asserted to GND and two states can be considered

(a) Voltage of ST node is low: when, voltage of ST node is low, the voltage of BL pulled down to low voltage by PMOS access transistor. We refer to this voltage of BL as VBL-Low.

(b) Voltage of ST node is height: when voltage of ST node is height, the voltage of BL and ST node equalized (we refer to voltage of BL in this state as VBL-High). Since in this state, there is very small different between BL and ST node, dynamic energy consumption is very small.

Idle mode: At the end of read operation, cell will go to idle mode and word-line2 and BL asserted to VIdle2 and V_{dd}, respectively.

2.4. 6T SRAM Cell

In this 6T memory cell as shown in Figure 2, the load is replaced by a PMOS transistor. This SRAM cell is composed of six transistors, one NMOS transistor and one PMOS transistor for each inverter, plus two NMOS transistors for access. This configuration is called a 6T Cell [5]. This cell offers better electrical performances (speed, noise immunity, standby current) than a resistive load 4T structure. The main disadvantage of this cell is its large size. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and ~BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, but both the signal and its inverse are typically provided in order to improve noise margins.

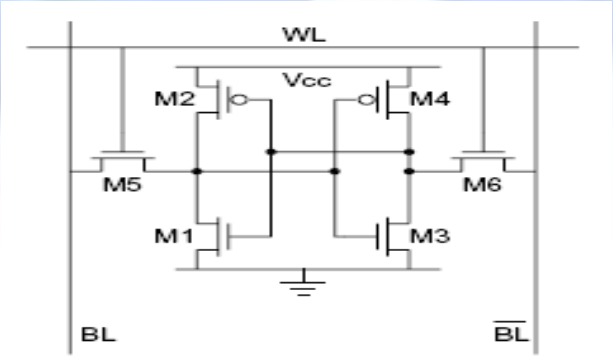

Figure 3 S-Edit Schematic of 6T SRAM Cell

2.4.1 Read Operation

Assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and ~Q are transferred to the bit lines by leaving BL at its pre-charged value and discharging BLB through M1 and M5 to a logical 0 (i.e. eventually discharging through the transistor M1 as it is turned on because the Q is Logically set to 1). On the BL side, the transistors M4 and M6 pull the bit line towards, a logical 1 (i.e. eventually being charged by the transistor M4 as it is turned on because Q is logically set to 0). If the content of the memory was a 0, the opposite would happen and BL would be pulled towards 1 and BL towards 0. Then these BL and ~BL will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has

higher voltage and thus will tell whether 1 was stored or 0. The higher the sensitivity of sense amplifier, the faster the speed of read operation.

2.4.2 Write Operation

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 0 and ~BL to 1. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily over ride the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

2.5 8T SRAM Cell

With the aggressive scaling in technology, substantial problems have been encountered when the conventional 6T (six transistors) SRAM cell configuration is utilized. This cell shows poor stability at very small feature sizes, the hold and read static noise margins are small for robust operation. Therefore, an extensive literature can be found on designing SRAM cells for low power operation in the deep sub-micron/nano ranges. The common approach to meet the objective of low power design is to add more transistors to the original 6T cell. An 8T cell can be found to solve the problem. This cell employs two more transistors to access the read bitline. The transistor configuration (i.e. M1 through M6) is identical to a conventional 6T SRAM cell. Two additional transistors M7 and M8 (thus yielding an 8T cell design) are employed in to reduce the leakage current.

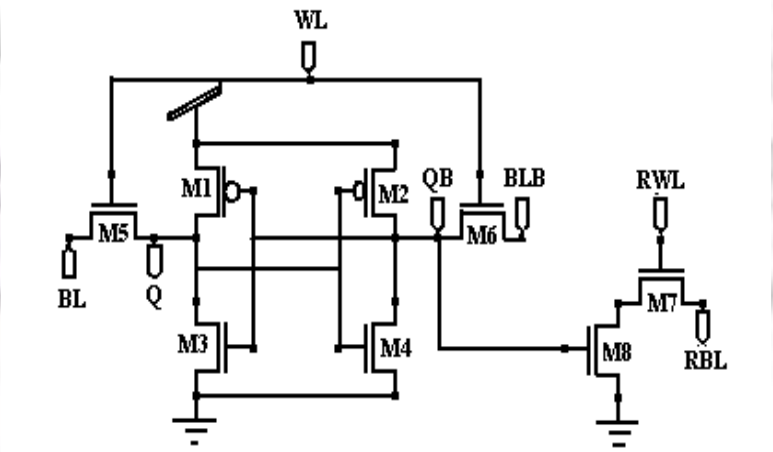

Figure 4: S-Edit Schematic of 8T SRAM Cell

To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation was proposed, for which separate read/write bit and word signal lines are used as shown in Figure 3.3, to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation. Write access to the cell occurs through the write access transistors and from the write bitlines, BL and BLB. Read access to the cell is through the read access transistor and controlled by the read wordline, RWL. The read bitline, RBL, is precharged prior to the read access. The wordline for read is also distinct from the write wordline. By doing this the worse-case stability condition encountered previously in a 6T SRAM cell, is avoided and high read stability is retained. However, for the 8T structure, the read bitline leakage is greater, especially in deep submicron/nano ranges. When the column for Read (RBL) is not accessed, the leakage current through M7 may cause a severe voltage drop at the read bit line, leading to large Power dissipation, thus error may appear at the output [8].

3. TANNER OUTPUT

We have taken here three circuits, i.e. 4T SRAM, 6T SRAM and 8T SRAM. Read and write operations of these three circuits are simulated in T-spice. Power dissipation is determined and compared for these circuits. We have used 90nm technology in this project to design the circuit.

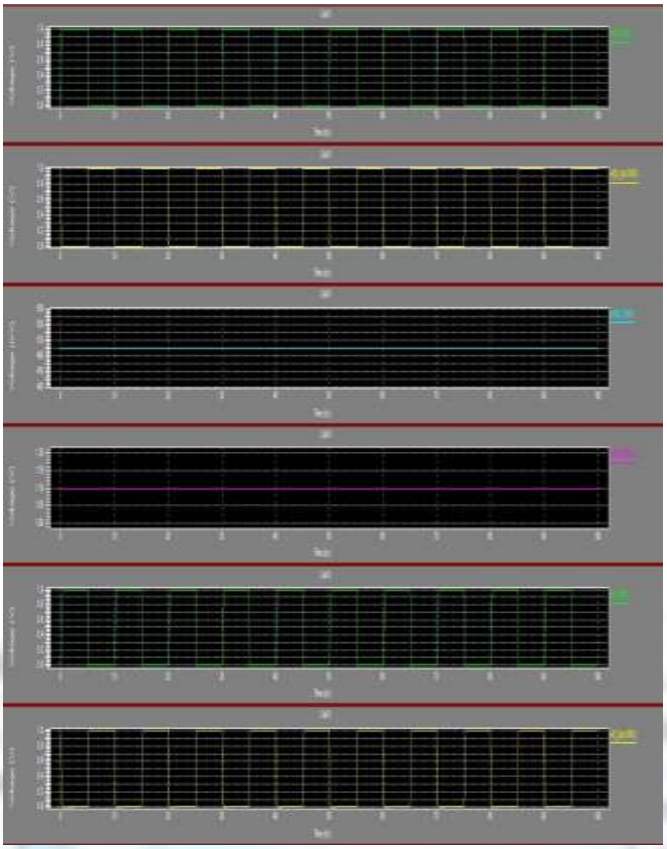

Figure 5 W-Edit Waveform of 4T SRAM Cell

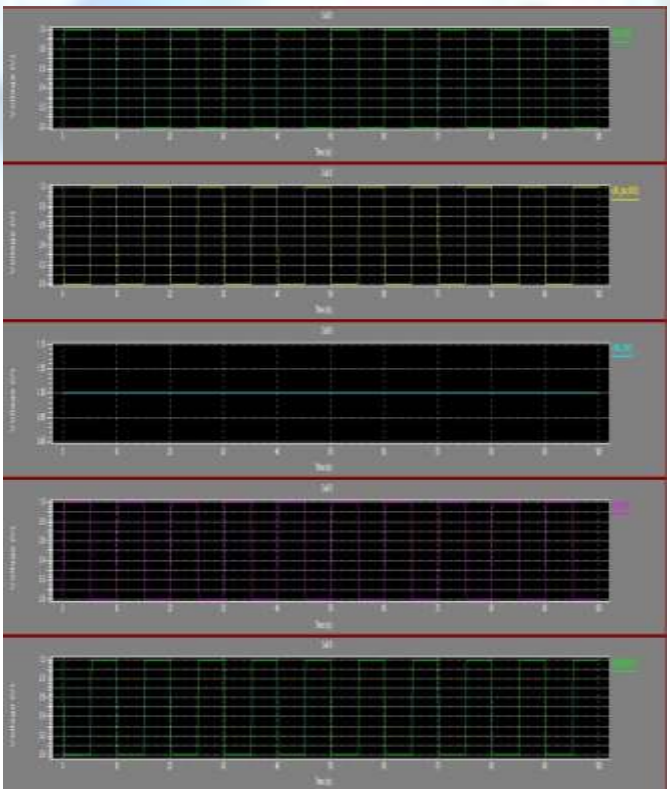

Figure 6 W-Edit Waveform of 8T SRAM Cell

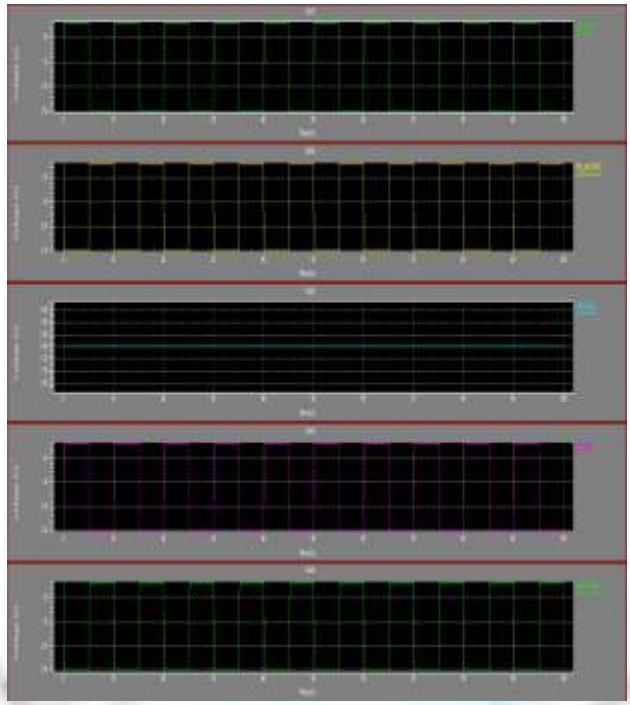

Figure 7 W-Edit Waveform of 6T SRAM Cell

4. RESULTS & OBSERVATIONS

We have simulated read and write operation of 4T, 6T and 8T SRAM Cell. Average power consumed and propagation delay by all the three different designs for the 32nm technology can be tabulated as below:

Effect of Variation of V_{DD} on Average Power Consumption

Average Power Consumption (µW)			
V_{dd}(Volts)	4T SRAM Cell	6T SRAM Cell	8T SRAM Cell
1	0.47	0.56	0.57
1.2	0.55	1.02	1.03
1.4	0.99	2.14	2.15
1.6	2.67	6.04	6.08

Table 1 Power with the variation of V_{dd}

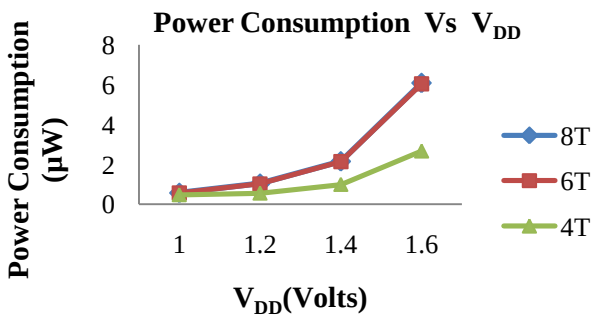

Figure 8 Variation of Power with Respect to V_{DD}

Effect of Variation of V_{DD} on Propagation Delay

Propagation Delay (ps)			
V_{DD}(Volts)	4T SRAM Cell	6T SRAM Cell	8T SRAM Cell
1	80.77	41.30	41.48
1.2	42.44	32.34	32.42
1.4	35.33	27.64	27.69
1.6	31.79	24.70	24.82

Table 2 Propagation Delay with the Variation of V_{DD}

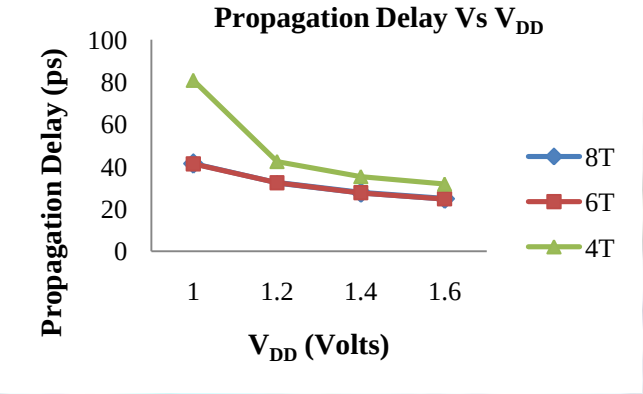

Figure 9: Variation of Propagation Delay with Respect to V_{DD}

5. CONCLUSION

A conclusion section must be included and should indicate clearly, the most efficient technique to reduce the average power consumption is the reduction of the supply voltage. From the above observation it is clear that 8T SRAM cell has higher power consumption than compare to 6T and 4T SRAM cell and also 4T SRAM cell has the least power consumption of the three. This is due to more number of transistor in 8T SRAM cell and secondly little complex working than the other one. The 4T SRAM cell takes 35.45% less cell area with respect to conventional 6T memory cell and consumes less power with respect to 6T conventional memory cell. In case of 4T SRAM cell, Least Power (0.47µW) shows at V_{DD} 1volt.

In case of Propagation Delay, after comparing the 4T, 6T and 8T SRAM cell, it is found that 8T SRAM cell provide a very low propagation delay (24.82ps) shows at V_{DD} 1.6 volt. The 8T SRAM structure uses the advantages of 4T and 6T SRAM, as 8T SRAM cell has a different read and write line.

6. REFERENCES

[1]. Sung-Mo Kang, Yusuf Leblebici," CMOS Digital Integrated Circuits Analysis and Design" TATA McGRAW HILL, Third Edition.
[2]. Neil H.E.Weste, David Harris and Ayan Banerjee "CMOS VLSI DESIGN – A Circuits and System Perspective "Pearson education, Third edition, ninth impression 2009, pp. 385.
[3]. Integrated Circuit Engineering Corporation "SRAM Technology" pp. 8.10-8.11
[4]. Ming-Long Fan, Yu-Sheng Wu, Vita Pi-Ho Hu, Chien-Yu Hsieh, Pin Su and Ching-Te Chuang," Comparison of 4T and 6T FinFET SRAM Cells for Subthreshold Operation Considering Variability—A Model-Based Approach," IEEE Transactions on Electron Devices, Volume 58, No. 3, March 2011, pp. 609-616.
[5]. Sushil Bhushan, Shishir Rastogi, Mayank Shastri, Shyam Akashe, Dr. Sanjay Sharma," High Density Four-Transistor SRAM Cell with Low Power Consumption," International Journal of Comp. Tech. Appl, Volume 2 (5), Spt-Oct 2011, pp. 1275-1282.
[6]. A. Goel, R.K. Sharma, A.K. Gupta," Process Variations Aware Area Efficient Negative Bit-Line Voltage Scheme for Improving Write Ability of SRAM in Nanometer Technologies," IET Circuits Devices Syst., 2012, Volume 6, Issue 1, pp. 45–51.
[7]. Lab Manuals for T-Spice, S-Edit and L-Edit
[8]. Nahid Rahman, B. P. Singh, "Design of Low Power SRAM Memory using 8T SRAM Cell," International Journal of Recent Technology and Engineering (IJRTE), Volume 2, Issue 1, March 2013, pp. 123-127.
[9]. V. Sharma, "SRAM Bit Cell Optimization," Springer Science & Business Media, New York 2013, pp. 09-30.