

# Design Analysis of Phase Locked Loops and its Applications

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## ABSTRACT

In this paper, the design analysis and applications of PLL based circuits has been discussed. The fundamentals of PLLs are introduced and a complete guide to analysis and simulation of a charge-pump phase-locked loop based clocking circuit at both behavioral as well as transistor levels is presented for use as a synthesizer in a serial link. Finally, a survey of potential future research areas to explore for both PLLs in high-speed links as well as the complete serial link is provided with an emphasis on signal integrity applications for future students pursuing graduate studies in the fields of Signal Integrity and Mixed-Signal IC Design.

**Keywords:** design, PLL, circuit, applications, analysis.

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## INTRODUCTION

A phase-locked loop or phase lock loop abbreviated as PLL is a control system that generates an output signal whose phase is related to the phase of an input signal. There are several different types; the simplest is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases matched.

Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis.

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

Frequency is the derivative of phase. Keeping the input and output phase in lock step implies keeping the input and output frequencies in lock step. Consequently, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. The former property is used for demodulation, and the latter property is used for indirect frequency synthesis. Phase-locked loops are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors.

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## BASIC DESIGN ANALYSIS OF VARIOUS PLLs

Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure. Both analog and digital PLL circuits include four basic elements:

- Phase detector,
- low-pass filter
- Variable frequency oscillator, and
- feedback path (which may include a frequency divider)

There are several variations of PLLs. Some terms that are used are analog phase-locked loop (APLL) also referred to as a Linear Phase Locked Loop (LPLL), Digital Phase-Locked Loop (DPLL), All Digital Phase-Locked Loop (ADPLL), and Software Phase-Locked Loop (SPLL) :

### Analog or Linear PLL (LPLL)

Phase detector is an analog multiplier. Loop filter is active or passive. Uses a Voltage-controlled oscillator (VCO).

### Digital PLL (DPLL)

An analog PLL with a digital phase detector (such as XOR, edge-trigger JK, phase frequency detector). May have digital divider in the loop.

### All digital PLL (ADPLL)

Phase detector, filter and oscillator are digital. Uses a numerically-controlled oscillator (NCO).

### Software PLL (SPLL)

Functional blocks are implemented by software rather than specialized hardware

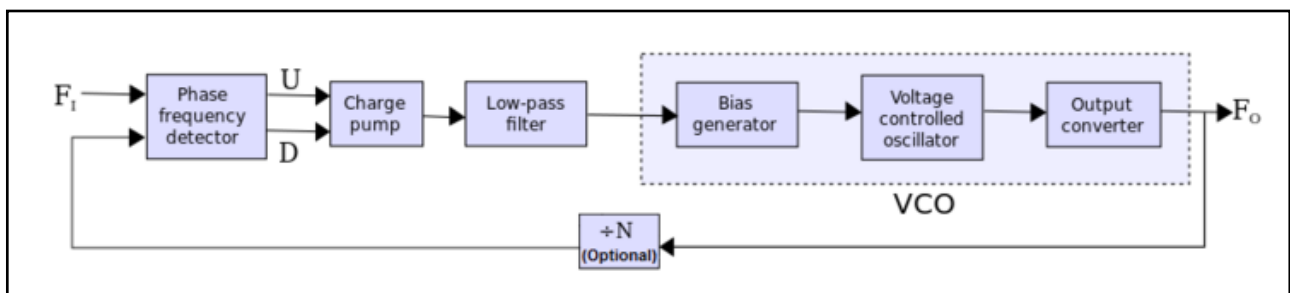


Figure 1: Block diagram of a Phase-Locked Loop

In Communication Systems I (ECE 4625/5625) you learn about the basic analog PLL for tracking the phase of a carrier signal:

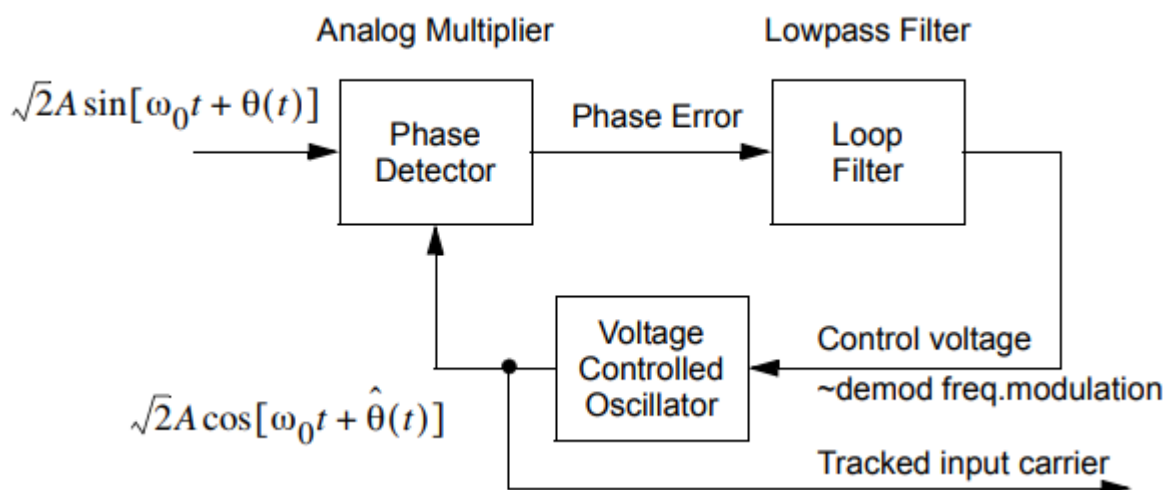


Figure 2: Basic analog PLL (APLL) for tracking the phase of a carrier signal

In simple terms the PLL as see above is a nonlinear feedback control system, which can be linearized under suitable assumptions – A big assumption for linearity to hold is that the loop is locked with a small tracking error

By inserting an analog-to-digital converter (ADC or A/D) the APLL can be moved into the discrete-time domain with a change of components:

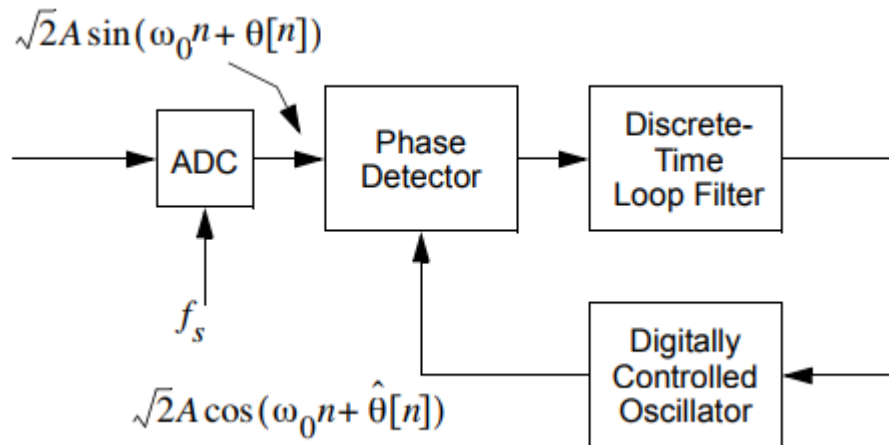


Figure 3: Basic digital PLL (DPLL) for tracking the phase of a discrete-time carrier signal.

Fundamentally the PLL is not restricted to carrier phase tracking.

When the PLL is used to track other waveform attributes, such as sampling instant under the control of an interpolator, or the time of delay of a locally generated waveform, as in spread spectrum, the PLL concept still holds:

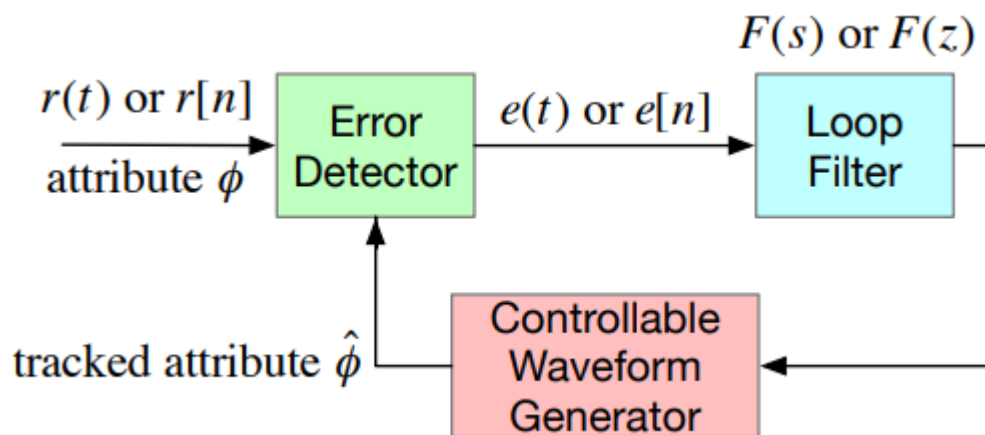


Figure 4: High-level PLL block diagram.

## APPLICATIONS OF PHASE-LOCKED LOOPS

Phase-locked loops are widely used for synchronization purposes; in space communications for coherent demodulation and threshold extension, bit synchronization, and symbol synchronization. Phase-locked loops can also be used to demodulate frequency-modulated signals. In radio transmitters, a PLL is used to synthesize new frequencies which are a multiple of a reference frequency, with the same stability as the reference frequency.

Other applications include:

- Demodulation of both FM and AM signals
- Recovery of small signals that otherwise would be lost in noise (lock-in amplifier)
- Recovery of clock timing information from a data stream such as from a disk drive
- Clock multipliers in microprocessors that allow internal processor elements to run faster than external connections, while maintaining precise timing relationships
- DTMF decoders, modems, and other tone decoders, for remote control and telecommunications

Various other applications of PLLs are:

### **Clock recovery**

Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery. In order for this scheme to work, the data stream must have a transition frequently enough to correct any drift in the PLL's oscillator. Typically, some sort of redundant encoding is used; 8B10B is very common.

### **Clock generation**

Many electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertz and the reference crystal is just tens or hundreds of megahertz.

### **Clock distribution**

Typically, the reference clock enters the chip and drives a phase locked loop (PLL), which then drives the system's clock distribution. The clock distribution is usually balanced so that the clock arrives at every endpoint simultaneously. One of those endpoints is the PLL's feedback input. The function of the PLL is to compare the distributed clock to the incoming reference clock, and vary the phase and frequency of its output until the reference and feedback clocks are phase and frequency matched. PLLs are ubiquitous—they tune clocks in systems several feet across, as well as clocks in small portions of individual chips. Sometimes the reference clock may not actually be a pure clock at all, but rather a data stream with enough transitions that the PLL is able to recover a regular clock from that stream. Sometimes the reference clock is the same frequency as the clock driven through the clock distribution, other times the distributed clock may be some rational multiple of the reference.

### **Spread spectrum**

All electronic systems emit some unwanted radio frequency energy. Various regulatory agencies (such as the FCC in the United States) put limits on the emitted energy and any interference caused by it. The emitted noise generally appears at sharp spectral peaks (usually at the operating frequency of the device, and a few harmonics). A system designer can use a spread-spectrum PLL to reduce interference with high-Q receivers by spreading the energy over a larger portion of the spectrum. For example, by changing the operating frequency up and down by a small amount (about 1%), a device running at hundreds of megahertz can spread its interference evenly over a few megahertz of spectrum, which drastically reduces the amount of noise seen on broadcast FM radio channels, which have a bandwidth of several tens of kilohertz.

### **Deskewing**

If a clock is sent in parallel with data, that clock can be used to sample the data. Because the clock must be received and amplified before it can drive the flip-flops which sample the data, there will be a finite, and process-, temperature-,

and voltage-dependent delay between the detected clock edge and the received data window. This delay limits the frequency at which data can be sent. One way of eliminating this delay is to include a deskew PLL on the receive side, so that the clock at each data flip-flop is phase-matched to the received clock. In that type of application, a special form of a PLL called a delay-locked loop (DLL) is frequently used.[9]

### **Frequency Synthesis**

In digital wireless communication systems (GSM, CDMA etc.), PLLs are used to provide the local oscillator for up-conversion during transmission and down-conversion during reception. In most cellular handsets this function has been largely integrated into a single integrated circuit to reduce the cost and size of the handset. However, due to the high performance required of base station terminals, the transmission and reception circuits are built with discrete components to achieve the levels of performance required. GSM local oscillator modules are typically built with a frequency synthesizer integrated circuit and discrete resonator VCOs.

### **Jitter and noise reduction**

One desirable property of all PLLs is that the reference and feedback clock edges be brought into very close alignment. The average difference in time between the phases of the two signals when the PLL has achieved lock is called the static phase offset (also called the steady-state phase error). The variance between these phases is called tracking jitter. Ideally, the static phase offset should be zero, and the tracking jitter should be as low as possible. Phase noise is another type of jitter observed in PLLs, and is caused by the oscillator itself and by elements used in the oscillator's frequency control circuit. Some technologies are known to perform better than others in this regard. The best digital PLLs are constructed with emitter-coupled logic (ECL) elements, at the expense of high power consumption. To keep phase noise low in PLL circuits, it is best to avoid saturating logic families such as transistor-transistor logic (TTL) or CMOS. Another desirable property of all PLLs is that the phase and frequency of the generated clock be unaffected by rapid changes in the voltages of the power and ground supply lines, as well as the voltage of the substrate on which the PLL circuits are fabricated. This is called substrate and supply noise rejection. The higher the noise rejection, the better. To further improve the phase noise of the output, an injection locked oscillator can be employed following the VCO in the PLL.

### **CONCLUSION**

This paper presents the design and analysis of Phase locked loops based circuits and its applications. PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CKref to produce a high-frequency clock CKout this is known as clock synthesis. A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant. A basic PLL is a negative feedback system that receives an incoming oscillating signal and generates an output waveform that exerts the same phase frequency relationship as the input signal. This is achieved by constantly comparing the phase of output signal to the input signal with a phase frequency detector (PFD).

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