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A Beginning in the Design of Reversible Barrel Shifter

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Abstract: One of the most important factors in designing VLSI devices is power consumption. The main advantage of reversible logic is that it reduces power consumption. In reversible circuits input vector can be determined from output vector in unique way. This means that for every input pattern, there is a unit output pattern. Loss of every bit of information leads to heat generation (energy release). Since no information is lost in reversible circuits, so no heat produced and energy is not released. Consequently, the power consumption is lower in reversible circuits. In fact, if a circuit is made of reversible gates, because of no information loss, it would not waste energy. In this paper a novel nanometric fault tolerant reversible barrel shifter is proposed. Our proposed fault tolerant reversible barrel shifter is the first attempt to design fault tolerant reversible barrel shifter. All the circuits have nanometric scales.
Keywords: Design, Barrel, Shifter.

INTRODUCTION

Reversible computing has got useful applications in the design of CMOS with low power consumption, Bioinformatics, optical information processing, quantum computing and nanotechnology-based systems. According to the researches, kTln2 joules of energy produce this account of heat, where k is the Boltzmann constant equal to $1.3806505 \times 10^{-23} m^2 kgs^{-2} K^{-1}$ (J / K) and T is the temperature of operation (Landauer, 1961). If the circuit is made of reversible logic gates, the circuit will not waste kTln2 joules energy content (Bennett, 1973). Reversible logic circuits do not waste energy because they do not lose information and the number of inputs and outputs is equal which results in one-to-one correspondence with each other (Kerntopf, 2004), i.e. not only outputs can be estimated from inputs uniquely but also the inputs can be retrieved from the outputs. Thus, the number of inputs and outputs in reversible circuits or logic gates are the same. Designing reversible circuits by reversible gates has got following restrictions (Hafiz Md., 2003):

1. Each signal has one fan out.
2. Feedback is not allowed.

BACKGROUND

To prevent energy dissipation in irreversible logic gates, reversible logic gates are proposed. There are a lot of reversible logic gates which we can note the most popular of them as Feynman gate (Feynman, 1985), Toffoli gate(Toffoli, 1980), Fredkin gate (Fredkin, 1982) and Peres gate (Peres, 1985) shown in Fig.1.

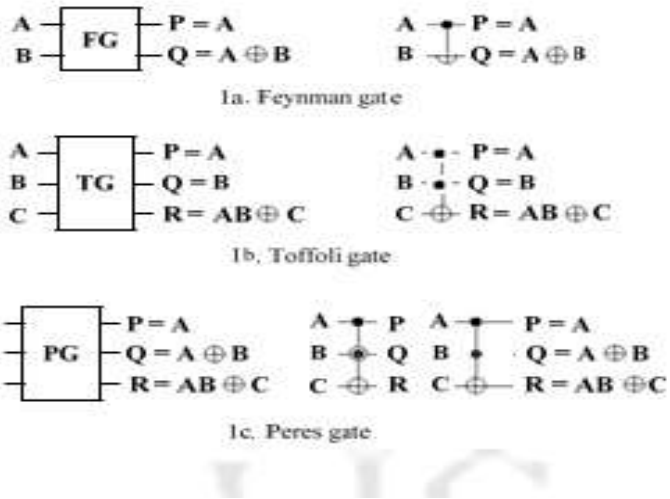

Fig. 1: Symbolic forms and block diagrams related to some of the famous reversible logic gates.

Every reversible logic design should minimize the following characteristics as possible (Islam, 2009):

Garbages: the output that is not used as primary output is called garbage output.

Constants: the input in input side of circuit that will be set to 0 or 1 is called constant input. Gate count: the number of gates used in the system should be minimal.

Hardware complexity: implies the main number of gates (NOT, AND, XOR gates) that is used for function blending.

Parity Preserve

Parity check is one of the oldest methods for detecting errors in digital systems which is used to detect errors in data storage or their transmission. The reason of this error is that the parity of data is not preserved by more arithmetic functions and other processor functions. So many attempts have been done to perform arithmetic operations on particular operands which in the parity check is executable. (Parhami, 2002; Parhami, 2002). On the other hand, such methods are not effective and need to develop more extensive. The truss tables corresponding to Feynman gate, Press gate and Toffoli gate have been shown in tables 1, 2 and 3 respectively.

Table 1: Truth table of Reversible Feynman Gate.

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 2: Truth table of Reversible Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 3: Truth table of Reversible Peres Gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Parity Preserving Reversible Gates:

When the parity of inputs and outputs is same, the reversible gate would be parity preserving. Mathematically a reversible gate

with n input lines and n output lines would be parity preserving if and only if:

$I_1 \oplus I_2 \oplus \ldots \oplus I_n \leftrightarrow O_1 \oplus O_2 \oplus \ldots \oplus O_n$

Which Ii and Oj are the input and output lines.

All gates are not necessarily parity preserving. We can prove that the gate is parity preserving by examining its truss table. Fault tolerance enables a system to continue its operations properly when error occurs in some parts of it. When the system is made of fault tolerant components error detection and correction is going comfortable. In communications and many other systems, parity leads to fault tolerance. Therefore, to develop nanotechnology, reversible fault-tolerant systems and parity preserving reversible circuits will be the most popular designs in the future. If all the constituent gates of design are parity preserving, the design will be parity preserving. Few parity preserving logic gates have been proposed so far which the most famous gates are F2G (Parhami, 2006), NFT gate (Haghparast, 2008) and FRG (Fredkin, 1982) which are shown in Fig. 2. FRG, F2G gates also are called one-through. This means one of the inputs is repeated identically in the output. If two of inputs are repeated identically in the output of the gate that gate is called two-through. For example, Toffoli Gate is two-through because two of the inputs have been repeated identically in the output.

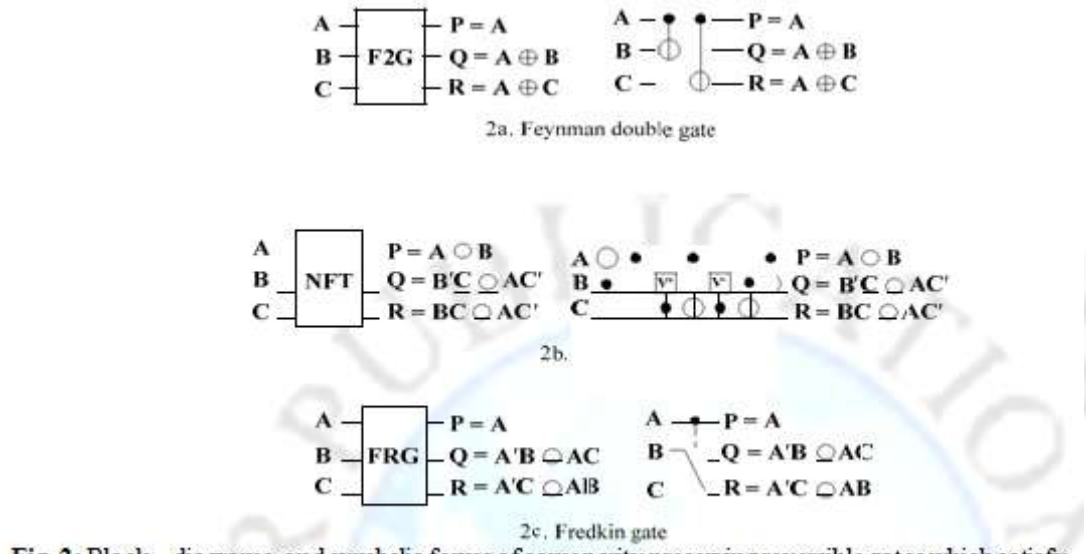

Fig. 2: Block diagrams and symbolic forms of some parity preserving reversible gates which satisfy A ⊕B ⊕C=P ⊕Q ⊕R.

The truth tables corresponding to Feynman double gate, NFT gate and Fredkin gate are shown respectively in tables 4, 5 and 6. All of these gates are parity preserving because they satisfy A ⊕B ⊕C=P ⊕Q ⊕R. Each k×k reversible logic gate which XOR of its inputs is equal to XOR of its outputs is parity preserving.

Table 4: Truth table of the parity preserving F2G gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table 5: Truth table of the proposed reversible NFT gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1

1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

Table 6: Truth table of parity preserving reversible FRG gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Conservative Gates:

Gates which in every row of its truth table the number of input 1s is equal to the number of output 1s. In other words, their Hamming weight is equal, if the gate is reversible. For example, Fredkin gate is conservative because it is reversible and in all rows of its truth table the number of input 1s is equal to the number of output 1s. If the gate is conservative it would be parity preserving and fault tolerant. Fig. 3 shows relationship between classes of reversible circuits which shaded regions indicate combinations of reversible logic subsets.

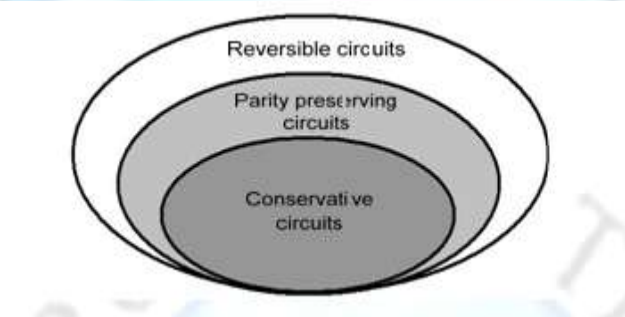

Fig. 3: Relationship between classes of reversible logic.

Reversible Barrel Shifters:

Shift and rotation are popular operations which are used in many applications such as address generation, variable length encoding, floating-point normalization, word pack/unpack, encryption and decryption algorithms, arithmetic operations and etc. Intel was the first company which used barrel shifters in their numerical data processors including programmable shifters that was able to shift any arbitrary number of bits or bytes per clock. Since then the barrel shifters were responsible for several patents due to various types of shifters. Several other combinational design patterns have been proposed for irreversible barrel shifters, but only two papers (Gorgin, 2007) and (Irina Hashmi, et al., 2010) have been published for reversible barrel shifter.

Fault Tolerant Reversible Barrel Shifter:

In this chapter, we introduce a new approach for designing fault tolerant reversible barrel shifter. On the other hand, one of most recent necessary operations in the computer tasks such as address decoding, computer arithmetic and logic operations is data shifting. There are several types of shift operations depending on their applications including logic shift, arithmetic shift and rotate. Our proposed fault tolerant reversible barrel shifter is the first endeavor for designing fault tolerant reversible barrel shifter.

Many of the peculiar and multipurpose arithmetic units used barrel shifter for data transfer. These shifters are the most common designs for choice due to high performance multi-bit transfer in a cycle. Barrel shifters have got many applications in high performance processors, test generation for digital signal processor, quantum cellular automata, high speed error control with low power consumption and etc. Typically barrel shifters are used in programs that have high speed and high performance. Thus, barrel

shifters are able to execute n-bit transfer and rotation in a cycle. Many techniques are offered for designing efficient barrel shifters in various fields.

New Fault Tolerant Reversible Barrel Shifter:

In this section, idea of a new fault tolerant reversible barrel shifter is proposed. Fault tolerance enables a system to continue its operations correctly when an error occurs in some parts of it. Detection and correction of errors is so convenient when the components of system are fault tolerant. In communication and many other systems parity will lead to fault tolerance. Therefore, the development of nanotechnology, fault tolerant reversible systems and parity preserving reversible circuits will be the most popular designs in the future. If all the gates forming design are parity preserving it will be parity preserving and parity preserving system will be fault tolerant. A reversible logic circuit design should be optimized for following criteria: minimum number of reversible gates minimum number of garbage outputs minimum number of constant inputs The minimum quantum cost of circuit Maintaining parameters above, we have proposed a new fault tolerant reversible barrel shifter. New circuit of new fault tolerant reversible barrel shifter is composed of reversible gates (Feynman double gate and Fredkin gate) which produce ten garbage outputs. Our proposal is shown in Fig.4. Circuit shows how we can apply Fredkin gate and Feynman double gate to combine parity preserving reversible barrel shifter.

CONCLUSION

In this paper we discussed about a new approach to design a fault tolerant reversible barrel shifter. The barrel shifters are able to shift data-words just in a single operation over the standard registers to the left or the right which are used in more than one clock. Barrel shifters are used in smaller devices too. Because they have speed advantage over than similar implemented software. A barrel shifter is a digital circuit that shifts a data-word with the given number of bits in a clock. It can be implemented as multiplexers and in such implementations output of a multiplexer is connected to the input of next multiplexer. In a way that is dependent on the shift distance. For example, consider a 4-bit shifter with inputs A, B, C, D. Shifter can rotate arrange of bits ABCD to DABC, CDAB or BCDA. In this case, no bit is lost, i.e. it can shift all outputs up to three positions to the right (And hence it builds any cyclic combination of A and B and C and D). The barrel shifter has many applications as it is become to account a useful component in microprocessors and ALU. All the scales are in the nanometric area.

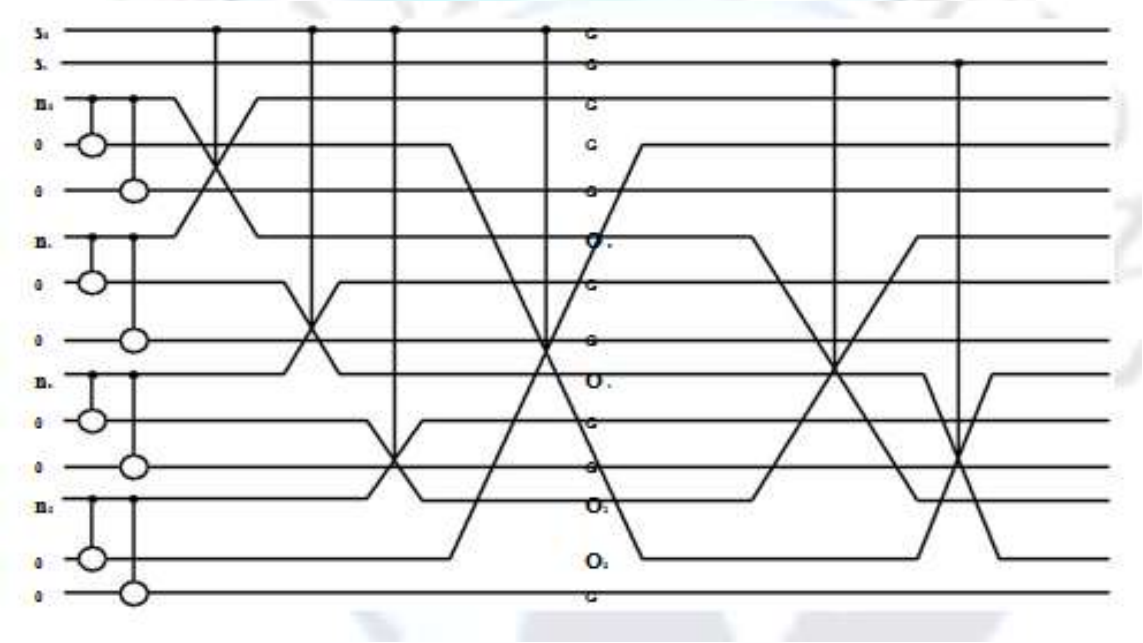

Fig. 4: Our proposed fault tolerant reversible barrel shifter.

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