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A quasi-Z-Source Modular Multilevel Converter with Overvoltage Blocking Capability: Experimental Validation

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ABSTRACT

This study assesses the performance of the quasi Z-source modular multilevel converter (qZS-MMC) in voltage boosting mode for medium voltage applications while also taking into account the design process and modulation of the device. The qZS-MMC is a modular multilevel converter (MMC) that enables the generation of an output voltage greater than the input DC voltage. It is made up of two quasi Z-source networks that are inserted between the two terminals of the DC input source and the DC-link terminals. Based on a mathematical derivation for the internal voltages, currents, and stored energy of the converter, two modulation techniques have been examined. It has been demonstrated that the quasi Z-source circuit gives the qZS-MMC half bridge sub-modules to handle DC-faults. The experimental findings support the effectiveness of the suggested modulation methods and the qZS MMC's capacity to block DC faults. The losses of the qZS-MMC are then contrasted with those of a typical MMC using full bridge sub-modules that also have DC fault capabilities. It has been determined in which range the qZS-MMC is more effective. Additionally, the qZS-MMC can offer a substantial reduction in the amount of semiconductor power devices while maintaining performance.

***Index Terms*—DC faults, half bridge sub-modules, modular multilevel converter, modulation schemes, quasi Zsource**

INTRODUCTION

ELECTRIC power systems are seeing an increasing Penetration of embedded generation, especially renewable energy resources such as wind turbines and photovoltaics [1-4]. The output voltage of most renewable energy sources fluctuates in a wide range with changes in the operating conditions. Therefore, having a power converter that can compensate for these fluctuations by being able not only to perform the more common voltage step-down, but also to step-up the voltage is desirable. Recently, a great attention has been paid to the modular multilevel converter (MMC) in both medium and high voltage applications due to its advantages of scalability, modular design, redundancy and better harmonic performance etc. [5-9]. The basic building block in an MMC is the sub- module (SM). There are different SM configurations that can be used. The most frequently used are the half bridge SM (HBSMs) and the full bridge SMs (FBSMs). The HBSMs are widely used to build the MMC [10-11]. However, a HBSMs-based MMC is unable to deal with DC- fault [12], thus depending on fast circuit breakers to isolate DC- faults. In addition, the peak value of the fundamental phase voltage is limited to one half of the total DC-link voltage levels (step-down operation). Therefore, the MMC with HBSMs must be upgraded with additional hardware to withstand the DC-fault currents and is considered inappropriate for interfacing many renewable energy sources to AC grid systems as it only works as a step-down converter. To overcome these shortcomings, using full-bridge SMs (FBSMs) instead of HBSMs has been proposed [13]. The resulting converter has an inherent DC-fault blocking capability as the FBSMs can insert both voltage polarities in the arm and block the overcurrent caused by short- circuiting the DC bus. Also, the output voltage range can be extended above the half value of the DC-bus voltage. These features are a result of the capability of the FBSMs to generate not only zero and positive voltage states as the HBSMs but also a negative voltage state. The FBSMs require as twice as many IGBTs as the HBSMs, which not only increases the converter cost, but also significantly increases the total power losses because the SM current flows through two IGBTs instead of one with the HBSMs [13].

An interesting solution can be achieved by combining HBSMs and FBSMs where depending on the ratio of the FBSMs to HBSMs, the DC-fault blocking and the voltage step- up capabilities of the FBSMs based MMC can be obtained [14]. For ratios that are equal to or higher than 1:1, the converter can block DC-faults. The ratio should be equal to or higher than 2:1 to extend the output voltage range (voltage step-up). This hybrid MMC has a limitation in its operation where the boosted output voltage should not exceed a specific value as this causes a capacitor voltage imbalance problem between the FBSMs and HBSMs. To clarify that, FBSMs can charge or discharge regardless of the arm current direction, while HBSMs can charge (discharge) only during positive (negative) state of the arm current. At a specific operating point, the negative current becomes insufficient to make the HBSM to discharge, which will lead to a steady voltage increase of the SMs capacitors of the HBSMs. It was reported in [14] that the maximum output voltage is restricted to 1.63 times of the half value of the DC- link voltage at unity power factor.

Due to the difficulties associated with the FBSMs based MMC and the hybrid MMC, a new approach based on integrating the impedance network concept [15-18] with the HBSMs based MMC proposed in [19], namely the quasi Z-source modular multilevel converter (qZS-MMC) is proposed in this paper. The qZS-MMC has the capability to step-up the output voltage and to block the DC-fault which is achieved by connecting the qZS capacitors with opposite polarity to the direction of the fault current. Two modulation schemes have been proposed in [20,21] focusing on the operation principles and derivation of the switches stress voltage. However, neither systematic design guidelines nor estimation of the capacitor stored energy/size have been provided in [20, 21]. Therefore, the two modulation techniques have been analysed in detail and validated experimentally in this paper.

This paper has been organized as follow. Section II presents the operation principles of the proposed qZS-MMC. The proposed modulation schemes are illustrated in Section III. Section IV provides a guideline for the capacitors and inductor design. Section V investigates the DC-fault blocking capability. The experimental studies are provided in Section VI to demonstrate the performance of the proposed converter. To highlight the advantages of the proposed converter, a comparison between the proposed converter, the MMC with FBSMs and quasi Z source cascaded multilevel converter is carried out in Section VII in terms of the required number of the passive and active components, total conduction and switching power losses and output voltage quality under similar input and output voltages and power levels. Finally, Section VIII concludes the work done in the paper.

QUASI Z-SOURCE MMC CIRCUIT CONFIGURATION AND OPERATION PRINCIPLES

Circuit Configuration

The structure of the single-phase configuration qZS-MMC is shown in Fig. 1. The MMC leg consists of the upper and the lower arms. Each arm is formed by *NSM* series-connected identical sub-modules (SMs), and an arm inductor (*LO*). Each SM is based on a half-bridge inverter configuration with one DC-link floating capacitor. The two switches (*S1* and *S2*) in the SM are controlled by a single state and its complement. When *S1* is on, the SM capacitor is bypassed, and the SM terminal voltage is zero. If *S1* is off, *S2* is on, therefore the voltage inserted by SM in the arm is equal to the SM capacitor voltage. Only during this latter active state, the capacitor gets charged or discharged according to the direction of the arm current [22], causing one of the limitations associated to the HBSMs. The quasi Z-source (qZS) stage consists of two identical qZS networks which are inserted between the DC source (*VDC*) and the MMC leg (or three-phase legs) as depicted in Fig. 1, where a single-phase configuration is shown. The two networks share a midpoint node "*O*" between the two capacitors *CU1*, *CN1* that can be used as a reference point for the output voltage *vAo*.

Summary of MMC Operation Principles

The desired AC output voltage is generated by changing the number of inserted SMs in each arm. The instantaneous voltage

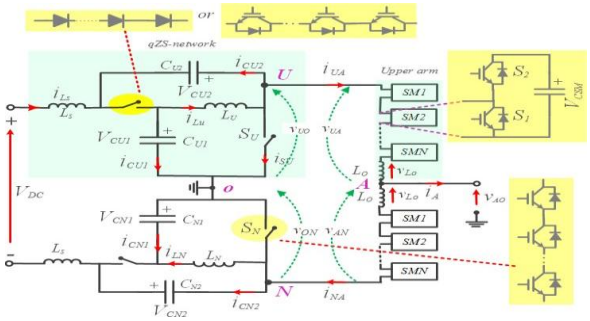

Fig. 1. Structure of a quasi Z-source modular multilevel converter

of the upper and the lower arms and the upper and lower DC- link voltages are denoted by v_{UA}, v_{AN}, v_{UO}, and v_{ON} respectively. By applying Kirchhoff's voltage law in Fig. 1, the AC output voltage is given by:

$$v_{AO}(t) = (v_{AN}(t) - v_{UA}(t))/2 + (v_{UO}(t) - v_{ON}(t))/2 \quad (1)$$

Assuming the direction of i_{UA} and i_{NA} is as shown in Fig. 1, the arm currents can be expressed by:

$$i_{UA}(t) = i_{AO}(t)/2 + i_{cir}(t), \quad (2)$$
$$i_{NA}(t) = -i_{AO}(t)/2 + i_{cir}(t)$$

where i_{cir} represents the circulating current in the arm. This current i_{cir} contains a DC component I_{UN} that provides the actual power transfer and AC components which usually contain even low order harmonics, with the second order one being the most significant. The circulating current i_{cir} and the second order harmonic component i_{2f} can be calculated by:

$$i_{cir}(t) = i_{2f}(t) + I_{UN} \quad i_{2f}(t) = (i_{UA}(t) + i_{NA}(t))/2 - I_{UN} \quad (3)$$

Summary of qZS Operation Principles

Similar to impedance-network circuits [17], the operation of the qZS requires the introduction of short circuit (shoot-through) at its output terminals in order to increase currents and consequently the energy stored in the qZS-network inductors which is later transferred to the qZS-network capacitors. This stored energy provides the voltage boosting capability [15].

It is difficult to use the MMC leg to produce the shoot- through by bypassing all the SMs in both the upper and lower arms due to presence of the arm inductors in the path of shoot- through current. The shoot-through path should have a low inductance. Even with the assumption that the arm inductors could be removed, bypassing all the SMs would lead to a drop in upper and lower arm voltage levels to zero, which would cause a high distortion in the output voltage and the benefit of having a multilevel functionality will be compromised. To prevent this, two chain-links of series connected switches S_U and S_N able to handle half the DC-link voltage are connected at the upper and lower qZS-networks end-terminals respectively to provide shoot-through current path to the DC-link midpoint "O" as shown in Fig. 1. The number of the series switches in each chain-link will be at least equal to the half number of SMs in each arm, assuming an equal voltage rating with the SMs switches. Generally, there are two operation modes for the qZS- network [15]. Considering the upper qZS-network which is shown in Fig. 2a, the operation modes are:

1) Shoot-through (ST) mode: The DC-link terminals are shorted, which forces the series diode to become reverse biased as shown in Fig. 2b. Hence, the stored energy in the capacitors begins to transfer into the inductors.

2) Non-shoot-through (NST) mode: The qZS-network is connected to the inversion stage then the series diode will be forward biased as shown in Fig. 2c. The stored energy in the inductors begins to transfer to the load, and qZS capacitors begin to charge.

During these switching modes, the SMs capacitor is charging or discharging depending only on the arm current polarity, where the SMs capacitor voltage decreases (increases) when the corresponding arm current is negative (positive) regardless of the switching modes.

Assuming the qZS components are identical where $C_{U1} = C_{N1} = C_1$, $C_{U2} = C_{N2} = C_2$, $L_U = L_N = L_S = L$ and consequently the capacitor voltages and inductor currents have their average value where $v_{CU1} = v_{CN1} = V_{C1}$, $v_{CU2} = v_{CN2} = V_{C2}$ and $i_{LU} = i_{LN} = i_{LS} = I_L$, the peak value of the DC-link voltages V_{UO}, V_{ON} and V_{UN} and qZS- network capacitor average voltages V_{C1} and V_{C2} are given by:

$$V_{UO} = V_{ON} = V_{UN}/2 = \frac{1}{1-2D_{sh}} V_{DC}/2 \quad (4)$$

$$V_{C1} = \frac{1-D_{sh}}{1-2D_{sh}} V_{DC}/2 \quad V_{C2} = \frac{D_{sh}}{1-2D_{sh}} V_{DC}/2$$

where D_{sh} is the ST duty ratio. Turning on any of the chain-link switches S_U or S_N causes distortion in the output

voltage levels which needs to be corrected by the SMs of the MMC stage using a suitable modulation technique and this will be further investigated in §III.

PROPOSED MODULATION SCHEMES

This section describes the proposed modulation schemes for qZS-MMC. The following assumptions were made when analysing the operating principles of the qZS-MMC:

- The qZS-MMC operates in inversion mode
- The SMs capacitor voltages in each arm are well balanced [22]
- The AC-circulating current is suppressed at a negligible level [23]
- The power losses of the converter are ignored

In this study, the phase disposition (PD) carrier technique is employed for the MMC with two opposite reference modulating signals for both the upper and the lower arm SMs. Assuming N_{SM} sub-modules are used per arm, N_{SM} level-shifted carriers are required and consequently, a (2 N_{SM} +1) level waveform is generated on the output. Each carrier is responsible for producing the gating signals of two SMs, one from upper arm and one from lower arm, which are chosen according to a capacitor voltage balance algorithm [22]. Through a switching frequency period, the total number of inserted SMs in the phase-leg are changed between N_{SM} -1, N_{SM} and N_{SM} +1 with total average of N_{SM}, hence:

$$v_{UA}(t) + v_{AN}(t) = v_{UN}(t) = N_{SM}V_C \quad (5)$$

From (1), the instantaneous value of the output voltage is

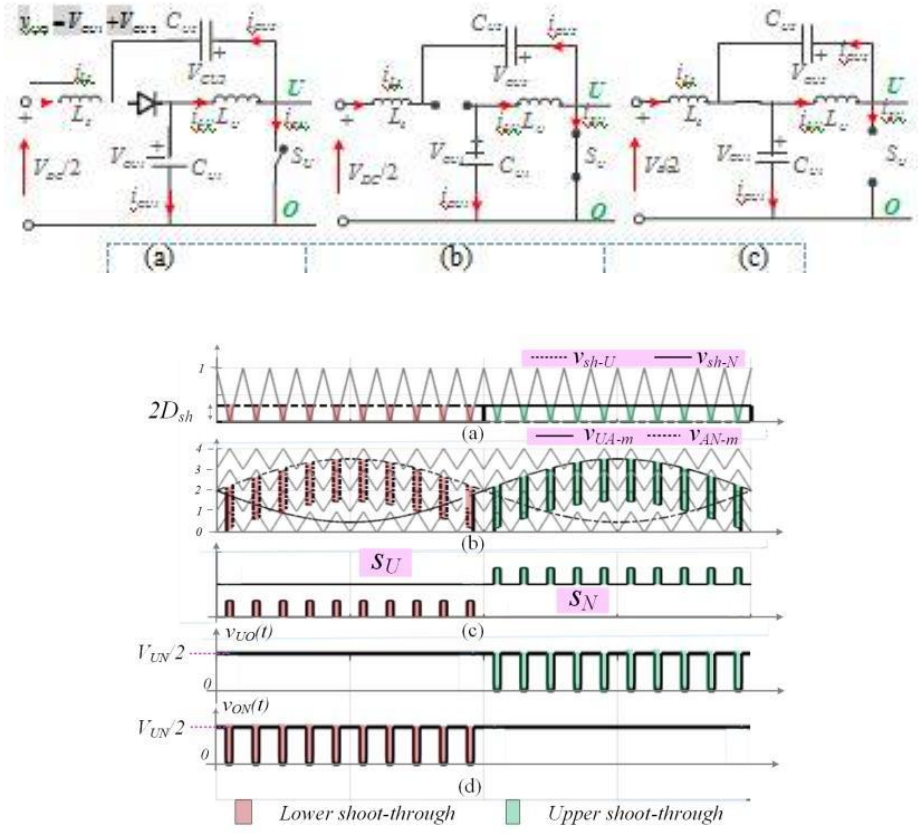

Fig. 2. RICs Modulation technique waveforms: a) ST modulation signals, b) Modified modulation signal, c) Chain-link switches pulses, and d) The upper and the lower DC-link voltages

DC-link voltage. The second term is because of product of the 1st order harmonic components of the upper arm current and the DC-link voltage. According to the power conversation law, the DC component in the arm current and the average value of the qZS-inductor current when using RICs technique are given by:

$$I = m_{RIC} I_m \frac{\cos\varphi}{4}, \quad I = \frac{mI_m \cos\varphi^{LN}}{4(1-2D)}$$

In this technique, since the SMs capacitor are charged according to the peak value of the DC-link voltage, the stress voltage on the chain-link switches becomes lower compared to the SS technique for the same output voltage.

The previous discussion is for a single-phase converter. However, for the three-phase converter, the three-phase legs are assumed to share the same DC-link connection points U and N as shown in Fig. 1. Due to dependence of the modulating signals for S_U and S_N on the polarity of the output voltage phase as shown in Fig. 4 when using RICs technique, if the upper chain- link switches are turned on, at least one of the upper arms in the three-phase legs will not be able to compensate the shorting of the upper DC-link terminals and that causes the output voltage of that particular leg(s) to decrease by maximum N_{SM} /2 voltage levels. Consequently, a significant distortion in the corresponding output phase voltage will be generated. To avoid causing any distortion in the three-phase output voltages when using the RICs technique, two qZS-networks are required for each phase-leg and connected to the same DC- -source terminals which results in a high number of components (6 qZS-networks) which leads to a more expensive and non- optimized converter. On the other hand, a half number of the SMs in each arm should be replaced by FBSMs, where the negative voltage polarity of FBSMs can been used to compensate the shorting of the DC-link terminals in case of number of inserted SMs lower than N_{SM} /2. This compensation mechanism is not the interest point of that paper.

The S_U and S_N are independent of the individual phase voltages when using SS technique for the single-phase converter. Therefore, for the three-phase converter the SS technique can be applied with only one qZS-network circuit (If the DC-side mid-point is not required).

Operation Constrains

As mentioned in §II.C, the upper and/or the lower qZS- series diodes will be forward biased during the interval of NST mode. However, during this interval, these diodes will be reverse biased if the following conditions are not achieved.

$$i_{Ls} + i_{LU} > i_{UA} \quad i_{Ls} + i_{LN} > i_{NA} \qquad (22)$$

where i_{LU}, i_{LN}, and i_{Ls} are the qZS-inductor currents with average value of I_L. If the instantaneous value of i_{UA} (i_{NA}) becomes higher than $2I_L$, the corresponding series diodes will be reverse biased in the NST mode. This leads to a drop in the peak value of the DC-link voltage to be V_{C1} instead of $V_{C1}+V_{C2}$ and causes a higher distortion in the output voltage. The limitation of the gain G can be deduced by substituting from (2), (9), (13), (19) and (21) into (22) for both techniques (at unity m and cosφ), which is:

$$G \geq 1.5 \qquad (23)$$

As is clear, to fulfil the conditions in (22), the gain value (G) should be higher than 1.5. For the gain less than or equal to one (in the buck mode), and a particular range of boost mode is $1<G<1.5$, the diodes become reverse biased in the NST mode and the output voltage will be highly distorted. To overcome this issue, a pair of active switches is added in anti-parallel with the diodes to provide a controllable path to the current in the reverse direction. Note that, the limit (23) is valid for single- phase converter. For the three-phase configuration (two qZS networks per three-phase leg §III.B), only SS technique can be applied. The gain limit is given by $G \geq 0.5$ (at unity m and unity cosφ). Therefore, the three-phase converter can work properly for most of the gain range without extra anti-parallel switches.

Control Scheme of the qZS MMC

There can be a considerable second order harmonic component in the circulating current i_{cir} particularly when the arm inductor size is small [23]. A proportional resonant (PR) controller $G_{PR1}(s)$ [23] is applied to eliminate the second order harmonic of the circulating current by following the undesired AC harmonic reference at the certain frequency (100 Hz) and then eliminate the steady state error. In addition, there may be imbalance in the value of passive components of the two qZS networks and also within HBSMs which unless compensated, causes a circulating fundamental frequency component current leading to imbalance of voltages produced by the qZS-networks and the two MMC arms, distorting the output voltage. To correct this, another proportional resonant controller $G_{PR2}(s)$ is applied to minimize the 50 Hz component in the circulating current caused by passive component imbalance. Fig. 5a shows the control block diagram including the two PR circulating current controllers discussed above.

The voltage balance control can be divided into 1) average
SMs capacitor voltage control and then, 2) SMs voltage balance control. Fig. 5b shows a block diagram of the average capacitor voltage control. The SMs average capacitor voltage is calculated by the summation of the upper and the lower cell capacitor voltages divided by $2N_{SM}$ which should be controlled by reacting to the circulating current reference. The outer loop forces the average voltage of the upper and the lower arms to follow the command voltage V^*.

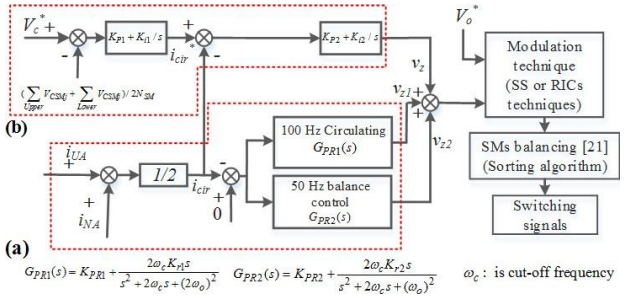

Fig. 3. Control block diagram including the circulating current control, the SMs capacitor average voltages control, the SMs capacitor voltage balance and arm balance control

Table I List of Parameters For The Qzs-Mmc Prototype

Parameter	Value	Parameter	Value
Peak output voltage (V)	170	qZS capacitances (mF)	3.3
Number of SMs per arm	2	Load resistance (Ω)	15.3
Arm inductance (mH)	2.5	Load inductance (mH)	2
SMs capacitances (mF)	3.3	Switching frequency (kHz)	10
qZS inductances (mH)	15		

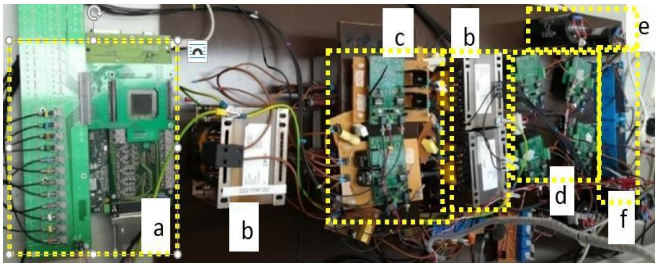

Fig. 4. Photograph of the experimental prototype, a) TMS320C6713 DSP and FPGA platform, b) qZS-inductors, c) qZS-switches, d) SMs switches, e) SMs capacitors, and f) arm inductors.

The control algorithm is implemented on a floating point 225- MHz TMS320C6713 DSP in charge of the calculations working in conjunction with an FPGA platform used for the A/D conversion of relevant voltage and current measurements and PWM signal generation. A daughter card is used for real-time data capture by a MATLAB host port interface (HPI). The experimental voltage and current waveforms are captured by a 200-MHz Lecroy oscilloscope whilst the control state variables are recorded in MATLAB through the HPI. The DSP sampling and the PWM carrier switching frequency are both set to 10 kHz.

A. Test 1: Verifying the Analytical Model of the qZS-MMC Circuit

The first test demonstrates the necessity of using the antiparallel active switches in qZS networks (S_{U1} and S_{N1}). The DC-supply voltage used is 280 V, D_{sh} was set to 0.15 and modulation index set to 0.98 to avoid the harmonics caused by working in the proximity of the over modulation region, which according to (8), results in an expected peak value of the output voltage of 167 V. the upper arm current i_{UA}, the upper qZS-inductor currents i_{LU} and i_{LS} and the upper DC-link voltage v_{UO}. To prove that equation (22) is satisfied, the summation of the two inductors currents (i_{LS} + i_{LU}) should be

compared to the arm current iUA. Fig. 12 shows that the zero crossing points of the channel Ch4 (iLS) and Ch2 (iUA) are the same and that the zero crossing of Ch3 (iLU) is set at the average value of the Ch4. It is therefore clear that when the waveforms of the arm current exceed the sum $iLS + iLU$, a negative current will be expected to flow through the diode which is impossible and therefore the arm current has to remain equal to $iLS + iLU$ which will cause a drop in the DC-link voltage as highlighted in that the arm current can be higher than $iUA + iLS$ without a drop of the DC-link voltage as a result of using active switches in antiparallel with the series diodes to provide a controlled reverse conduction path.

The output voltage and current and their harmonic spectrums for the two cases are respectively. The scope data of the output voltage and current is extracted and used to display their FFT. The peak value of the fundamental output voltage as revealed by the FFT is 163 V. The difference between the expected peak value of the fundamental output voltage (167 V) and the actual measured one (163 V) is caused by voltage drops on qZS inductors and the power semiconductor devices. Even though the converter delivers approximately the same fundamental voltage and current (in amplitude) in both cases, using only the series diodes resulted in significantly higher level of low order harmonics (3^{rd}, 5^{th} and 7^{th}). This distortion is also revealed by the differences in the total harmonic distortion (THD) values for the output voltage and current that are 19% and 8.5% respectively when using only the series diodes compared to 12% and 4.3% respectively when using also the antiparallel switches.

In another test, the performance of SS and RICs techniques has been compared. The DC-source voltage was set to 225 V with converter modulation index of 0.98 and a ST duty ratio of 0.25 and 0.17 was used with the SS and RICs respectively to obtain the same voltage gain value (G = 1.48), with an expected peak of the fundamental output voltage being 167 V. However, the peak value of the fundamental output voltage is equal to 162.5 V. The upper and the lower DC-link voltages (vUO and vON), and qZS- capacitor voltages ($vCU1$ and $vCN1$) are shown in Fig. 5. The peak values experienced in the DC-link voltages for SS and RICs techniques are 225 V and 170 V respectively and the qZS-capacitor average voltages are 169 V and 140 V respectively. Therefore, it is demonstrated that the stress voltage on the chain-link switches and the qZS-capacitor voltage rating are high for the SS technique compared to the RICs technique. The upper and lower arms SMs capacitor voltages that are captured by MATLAB HPI are shown in Fig. 16 for both techniques. It is noted that both cases have the same average capacitor voltage which is 168.5 V despite different DC-link peak voltages. The peak to peak capacitor voltage ripple in case of RICs technique is 86% of that for SS technique which agrees with the design prediction in Fig. 6 at a gain value of 1.5. The upper and lower qZS-inductor currents and source current are shown in Fig. 7 for both modulation techniques. It is noted that the inductor currents iLU and iLN have a high ripple at fundamental frequency in case of using RICs technique where their peak equals

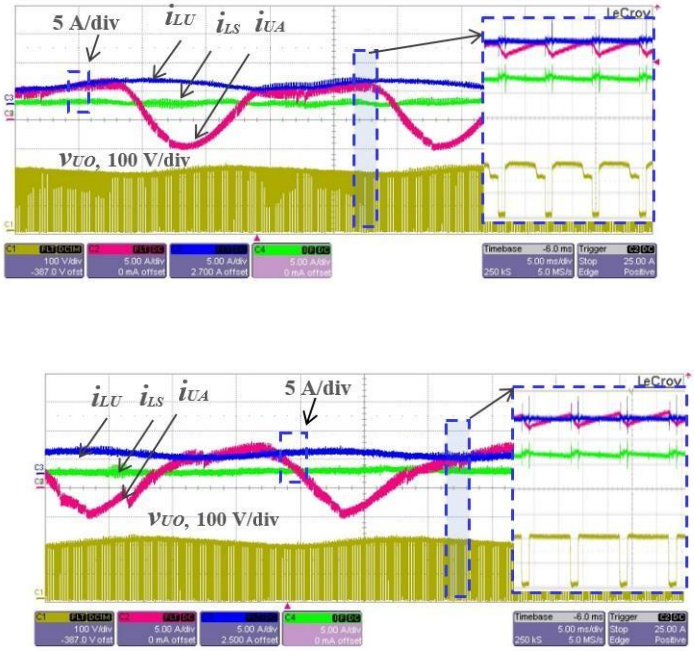

Fig. 5. Experimental results at D_{Sh} = 0.15 and V_{DC} = 280V when using a) series diodes only, b) antiparallel switches with diodes, which including, iLS : source current (5 A/div); iUA : upper arm current (5 A/div); iLU : upper qZS-inductor current (5 A/div); vUO : upper DC-link voltage (100 V/div)

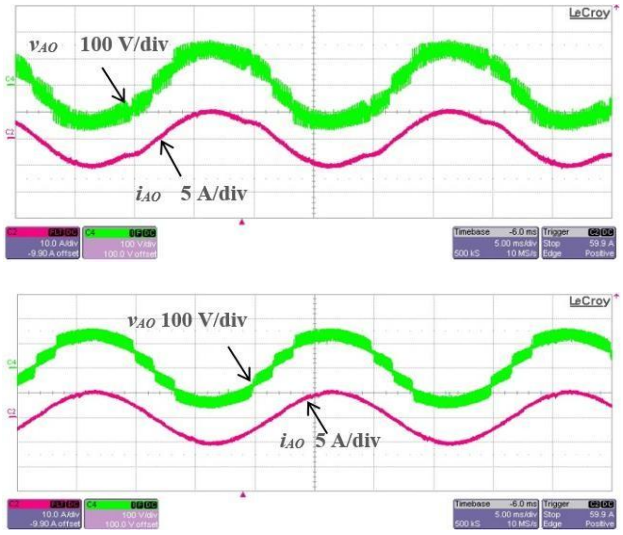

Fig. 6. Experimental results including output voltage and currents: a) series diodes only, b) antiparallel switches with diodes. Including, *iAO* : load current (5 A/div); *VAO*: output voltage (100 A/div)

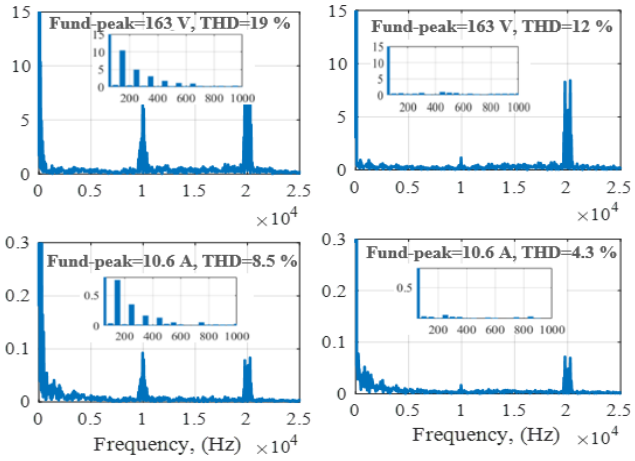

Fig. 7. Output voltage (top) and current (bottom) FFT: a) series diodes only, b) antiparallel switches with diodes

Since the stress voltage on the chain-link switches in the case of using the SS technique is high compared to RICs technique, and also applying only partial ST intervals of RICs as illustrated in Fig. 8 (i.e. half switching frequency), the qZS- networks losses are higher when using SS technique compared to RICs technique. Fig. 8 has been added which indicates the experimental efficiency curves of the reduced scale qZS-MMC prototype according to the output power variations in both techniques RICs and SS techniques at gain value equals 1.6. The output power is adjusted by changing the load resistance value while the output voltage is kept constant. The input power was measured by reading the voltage and current readings delivered by the power supply whilst the output power was calculated by measuring the load current and then by knowing the load resistance, apply the I^2R power relation. Using RICs technique makes the converter has a higher efficiency compared to SS technique.

Test 2: Operation Under DC Fault

To assess the response of the proposed qZS-MMC to a pole- to-pole DC-side short-circuit fault, an AC supply has been added at the AC output terminals of the qZS-MMC. The DC fault has been implemented by using a contactor in series with a 2 Ω resistor to limit the fault current to a relevant level for such a test; this sub circuit has been inserted between points X and Y as shown in Fig. 10. The DC supply voltage is set initially at 100 V and reduces quickly by 90% once the fault occurred due to the maximum current limitation of the DC voltage supply as shown in Fig. 19a.

The supply voltage, the grid voltage, the grid current and the lower arm current are shown in Fig. 19a. The controller detects the fault by monitoring the DC-side current (iLs) such that this current is reversed and rapidly increases

exceeding an overcurrent threshold current level of -I_L when the fault occurs. Once the fault is detected, all IGBTs are turned off. After the IGBTs are blocked, the grid current and the lower arm current fall directly to zero as shown in Fig. 19a. The inductor current i_{Ls} oscillates following a natural resonance as shown in Fig. 8b until it settles to zero which coincides with an absolute peak overshoot current of approximately 2.2 times the operating current from steady-state condition. Although this value may be considered high, it should be noted that the resonant current only flows through the inductors and the capacitors of the qZS-networks and this current does not flow through the chain-link switches *SU*, *SN*, *SU1* and *SN1* as has been discussed in §V. The chain-link switch current i$_{SU}$ is indicated in Fig. 9b. The qZS-capacitors *C1* and *C2* start to discharge and charge respectively until their voltages become approximately equal as illustrated in Fig. 9c (Ch2 and Ch3 have the same zero crossing position), whereas the SMs capacitor voltages are kept mostly unchanged. To conclude, these results verify the DC-fault blocking capability of the proposed qZS-MMC.

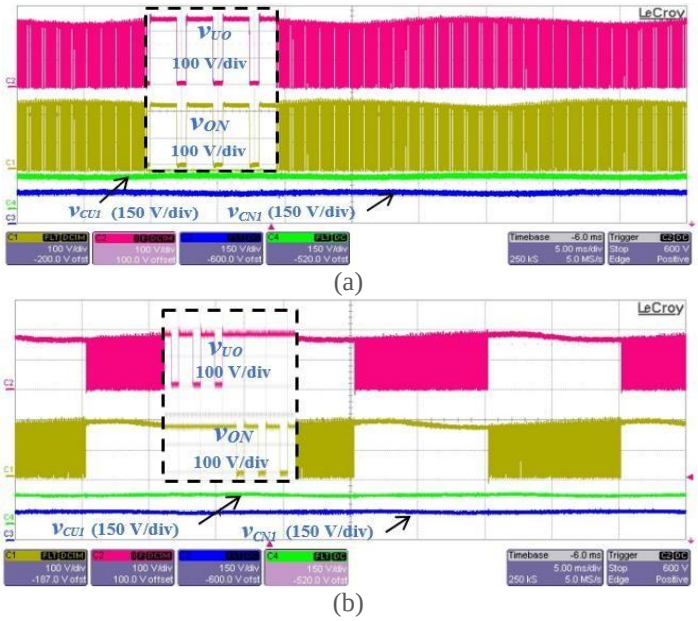

Fig. 8. Experimental results including the upper and the lower DC-link voltages *vUO* and *vON* (100 V/div), and qZS-capacitor voltages *vCU1* and *vCN1* (150 V/div) for, a) SS technique and, b) RICs technique

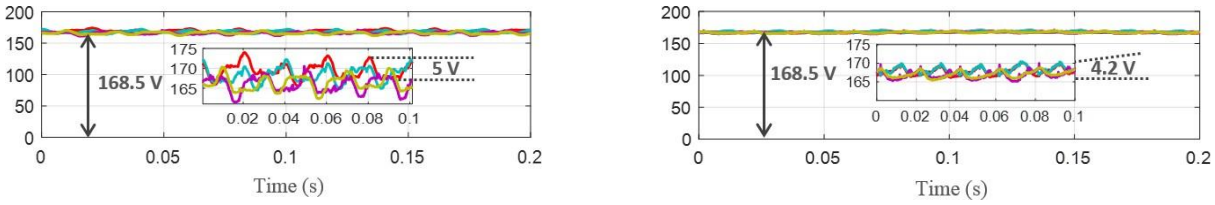

Fig. 9. Experimental results captured by MATLAB via the HPI of the upper and lower arms SMs capacitor voltages for, a) SS technique and, b) RICs technique

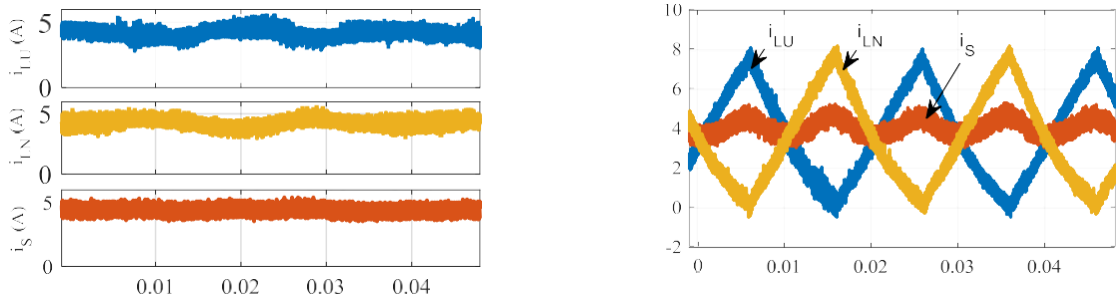

Fig. 10. Experimental results including the upper and the lower qZS-inductor currents *iLU* and *iLN* and source current *iLs* for, a) SS technique and, b) RICs technique

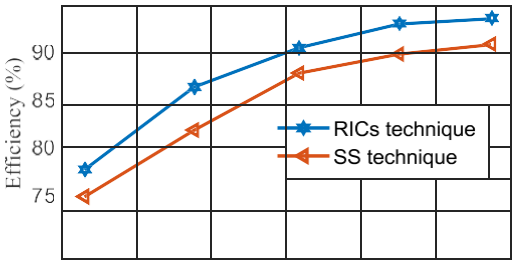

Fig. 11. Efficiency comparison of the prototype when using RICs or SS techniques at G = 1.6

TOPOLOGIES COMPARISON

In the previous section, the attractive features of the proposed qZS-MMC have been showcased which make it suitable for use in medium voltage/power wind turbines and/or photovoltaic generation systems. It is interesting to compare the proposed converter with the MMC based on FBSMs (FB-MMC) [25] and

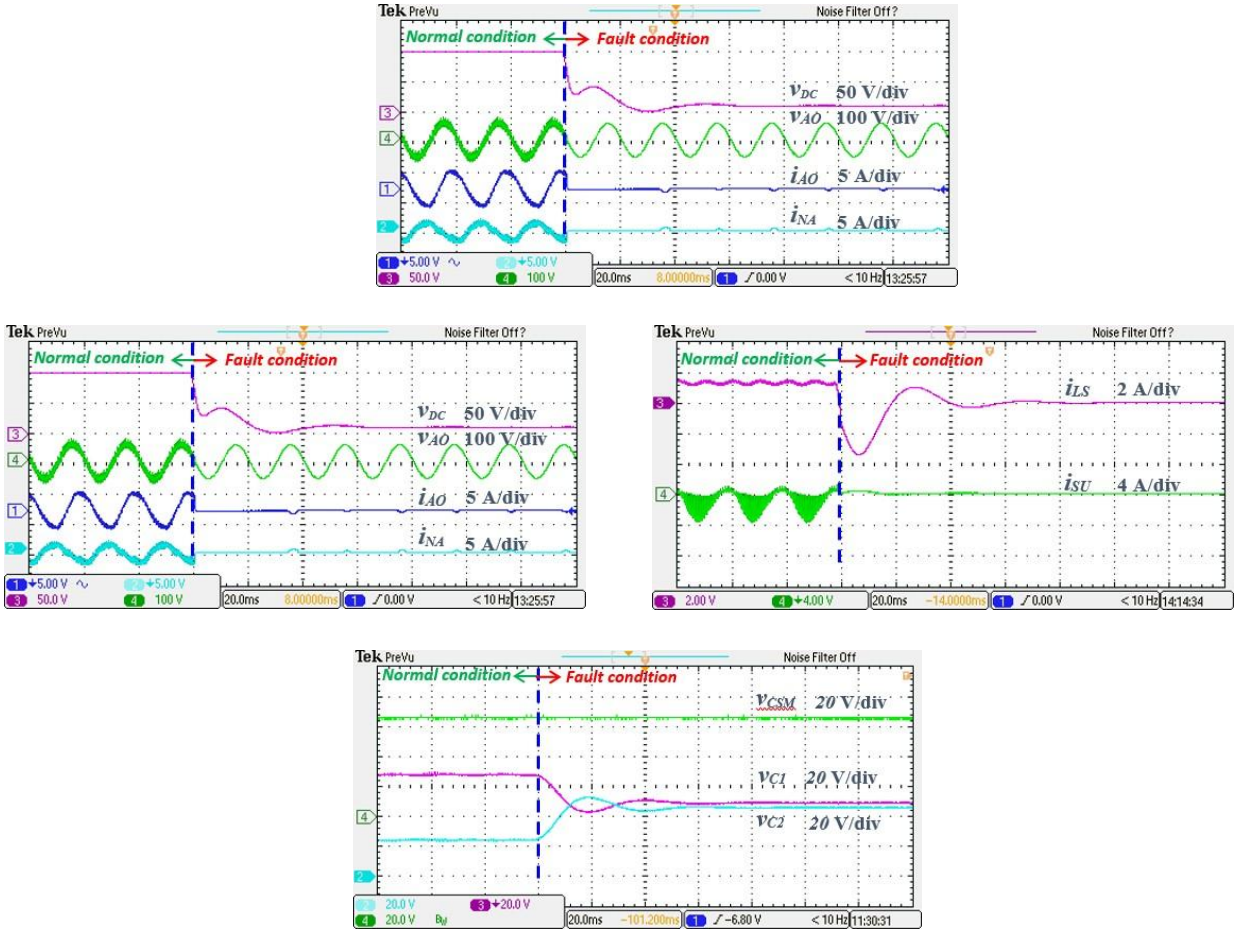

Fig. 12. Experimental results of the DC-fault: a) DC-voltage vDC (50 A/div), grid voltage vAO (100 A/div), grid current iAO (5 A/div), and arm current iNA (5 A/div), b) source inductor current iLS (2 A/div) and qZS switch current iSU (4 A/div), c) SM capacitor voltage $vCSM$ (20 A/div), qZS capacitor voltages $vC1$ and $vC2$ (20 A/div)

quasi Z-source cascaded multilevel converter (qZS-CMI) [26] as they both are able to provide voltage boosting capability. The comparison has been carried out in terms of number of passive and active components, conduction and switching power losses and output voltage quality for the same output voltage level. The case study of a 6.6 kV, 5 MW wind turbine generation system as described in [25] has also been considered in this paper.

Number of Components

The comparison here is carried out in terms of the required number of semiconductor devices, inductors, capacitors and DC voltage sources for the same amplitude of output AC voltage in both single-phase and three-phase implementations. The peak value of output phase voltage was fixed to 5.4 kV, then the gain *G* is set to 2 to get the required source voltage which is 5.4 kV. Regarding the proposed converter, considering four SMs per arm, each SMs needs to have an average capacitor voltage equal to 2.7 kV. According to (9), and (19), the duty ratio needs to be set to 0.25 and 0.33 for RICs and SS techniques respectively. As a result, the required DC-link voltage is 10.8 kV and 16.2 Kv respectively. Considering the same voltage rating for both SMs and qZS-networks devices, 2 devices rated at 3.3 kV per chain- link are required when using the RICs technique while 3 devices per chain-link are required for the SS technique. Taking the number of the IGBTs in FB-MMC as a reference, the total number of IGBTs required by r the qZS-MMC with RICs and SS techniques reduces to 75 % and 87.5 % respectively, and to 62.5 % for qZS-CMI in the case of single-phase converter. For a three-phase converter implementation, due to the fact that the qZS switches are shared with the other two phases, the number of IGBTs required by the qZS-MMC controlled by the SS technique decreases to 62.5% which is considered a significant reduction in terms of number of semiconductor power devices while it is 83% for qZS-CMI,. It should be noted that a convenient three-phase implementation is not possible for the qZS-MMC with RIC. Table II summarizes the relevant steps in defining the power semiconductor requirements, inductors and capacitors and DC voltage sources.

Losses Comparison

To have a fair losses comparison of the proposed converter with the FB-MMC [25] and qZS-CMI [26], it is mandatory to evaluate the losses using the same power semiconductor devices. To attain nine-level of the output voltage, 4 SMs per arm for both the proposed converter and FB-MMC and 4 cascaded SMs (full-bridge (FB) with qZS-networks) for qZS- CMI. Hence, 3.3 kV voltage rating IGBTs can be used, such as the 5SNA0800N330100 device to be used in the SMs and the chain-link switches. The estimation of the switching losses model relies on the switching energies stated in the device datasheet which are characterised by the manufacturer at an operating temperature of 125 which is then transferred in the generic PLECS thermal model. The FB-MM is modulated using phase disposition PWM (PD-PWM) [6], while the qZS- CMI can be only modulated using phase-shift PWM (PS-PWM) technique [26]. The frequency of the triangular carrier signal f_c is chosen to be 4 kHz for qZS-MMC and FB-MMC whilst the actual average number of commutations per second per SMs is shown in Table II. To make the comparison more credible, the PS-PWM technique used for qZS-CMI is adjusted to achieve the same number of transitions as that of PD-PWM, by setting the carrier frequency to 1 kHz for the cascaded units in this case. It is worth to mention that the resulting shooting-through frequency is 2 kHz for qZS-CMI and 4 kHz for the qZS-MMC. Table III shows the total conduction losses and switching losses in SMs and qZS-networks and the total converter losses for each of the converter candidates and operating mode. As expected in boost mode (at gains 1.25, 1.5 and 2), RICs technique adds more SMs switching losses compared to the SS technique. This is a result of having to turn on/off NSM /2 of SMs during ST intervals that leads to an average switching frequency $3fc/NSM$ which is three times higher than in the case of using the SS technique (fc/NSM). However, the stress voltage on the chain-link switches is higher in the case of using the SS technique compared to RICs technique and by applying only partial ST intervals of RICs (Fig. 4), the qZS-networks losses are higher when using SS technique especially with increasing the gain. Due to FBSMs having two switches in the current path rather than one in the HBSMs, the FB-MMC gets higher SMs conduction losses compared to qZS-MMC which is up to three times more at higher voltage gain. In qZS-CMI, as a result of having to use the FB switches for implementing the shoot through, the qZS-CMI gets higher SMs conduction and switching losses.

In the buck mode, the qZS-MMC and qZS-CMI have lower total losses compared to the FB-MMC at gain equal to 0.7. In boost mode, the FB-MMC has lower total losses (65% - 70%) compared to the qZS-MMC with RICs, while the qZS-CMI and qZS-MMC that use the SS technique have approximately equal total losses. However, if the shooting through frequency for qZS-MMC is adjusted to be equal to the shooting through frequency of qZS-CMI, the qZS-MMC will be more efficient compared to qZS-CMI. To conclude, the FB-MMC converter is more efficient compared to qZS-MMC with RICs in boost mode especially when increasing the gain, where 2.2% total losses percentage for FB-MMC compared to 3.2% total losses percentage for qZS-MMC with RICs at *G* equals 1.5. However, the qZS-MMC and qZS-CMI are more efficient in buck mode with losses percentage equal 2.4% and 2.2 % respectively, compared to 2.9 % for FB-MMC at G = 0.7.

Comparison of PWM Harmonics Profile

The harmonic spectrum of the phase voltage of the FB- MMC, qZS-CMI and qZS-MMC are compared and shown in Fig. 20 for different gains (1, 1.5 1.75, and 2). The SS and RICs techniques produce the same harmonic profile, therefore, the harmonic profile has been shown for the RICs technique only. It is noted that the switching harmonics of qZS-MMC with the two techniques appear as sideband clusters at the carrier frequency where the most dominant harmonic cluster

is located at twice the carrier frequency (8 kHz) for all gain values. The harmonic profile of the FB-MMC at gain equals 1 and 2 is similar to the qZS-MMC. However, at intermediary gain values, an additional dominant harmonic cluster appears for FB-MMC at the carrier frequency. This is an important finding since a larger harmonic cluster at lower frequency will require an increased size for the filter. The switching harmonics of qZS-CMI appear as sideband cluster at twice the carrier frequency (8 kHz) for all gains. The total harmonic distortion THD of the output voltage of the qZS-MMC and FB-MMC is approximately equal to 9.2% and 8.7% for all gain values respectively. For qZS-CMI, the THD equals 15%, 18.2%, 23.3%, and 23.5% for the gain values of 1, 1.5, 1.75, and 2 respectively. This is because in order to increase the gain of qZS-CMI, the modulation index should decrease with increasing the shoot through duty ratio which leads to a drop in the output voltage level, while the modulation index could remain fixed for all gains for the other converters.

CONCLUSIONS

For two suggested modulation schemes, a precise mathematical model of the quasi Z-source modular multilevel converter (qZS-MMC) has been developed. Investigated and discussed is how the suggested converter performs with the two modulation approaches simultaneously shorted (SS) and reduced inserted cells (RICs). Analysis and comparison of the capacitor voltage ripple in the qZS-networks and the MMC sub-modules for the two modulation approaches provides an estimation of the necessary capacitor energy.and sizes. The ability of the proposed converter to block the DC-fault current has been investigated. A small-scale laboratory system has been built and has been used to demonstrate the performance of the proposed converter and its capability to handle the DC-fault. Additionally, a comparison of the proposed converter's component count, total conduction and switching losses, and output voltage quality has been made with the MMC with complete bridge sub-modules and pseudo Z-source cascaded multilevel inverter. The proposed qZS-MMC controlled by the SS approach requires between 62.5% and 75% less IGBTs than MMC with full bridge or qZS-CMI, which is a substantial reduction. In terms of semiconductor device losses, the qZS-MMC is more efficient in buck mode of the output voltage at the switching frequency, which will either need expanding the filter or tripling the switching frequency. In the latter, the losses could rise to a level where the MMC loses efficiency in comparison to the suggested qZS-MMC. Comparing the qZS-CMI to the qZS-MMC and the MMC with full bridge, the THD of the qZS-CMI is higher, especially as the gain is increased.

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