International Journal of Enhanced Research in Science, Technology & Engineering
ISSN: 2319-7463, Vol. 11 Issue 12, December-2022, Impact Factor: 7.957

A Family of Multiport Switched-Capacitor Multilevel Inverters Is Used To Distribute High Frequency AC Power

Mr. G. Purushothaman[1], Mr. K. Nateshwaran[2], Dr. R. Arulmozhiyal[3], Mr. M. Bharanidharan[4]

[1,3,4]Assistant Professor, Electrical and Electronics Engineering, MAM School of Engineering
[2]PG Student, Electrical and Electronics Engineering, MAM School of Engineering

ABSTRACT

In order to distribute high frequency AC power, this research suggests a family of multiport switched-capacitor multilevel inverter (SCMLI) topologies. It uses asymmetric DC voltage sources with a common ground, which makes it perfect for use in modern electric vehicle factories and renewable energy farms. In comparison to numerous current topologies, the suggested family of step-up SCMLI achieves a higher number of output voltage steps with an optimal component count. The capacitors are naturally charged to a finite voltage every half cycle, which solves the problem of capacitor voltage balancing. A thorough analysis of two staircase modulation strategies—selective harmonic elimination and lowest total harmonic distortion—is presented together with research on how switching angles and THD change as a function of modulation indices for each strategy. For the proposed family of topologies, the working principle and analysis are described. Under both of the aforementioned modulation strategies with equal and unequal output voltage waveform steps, simulation findings are validated with experimental data.

***Index Terms*—H-bridge, HFAC power distribution, high frequency DC/AC Inverter, multilevel inverter, selective harmonic elimination, pulse width modulation, switched- capacitor, total harmonic distortion**

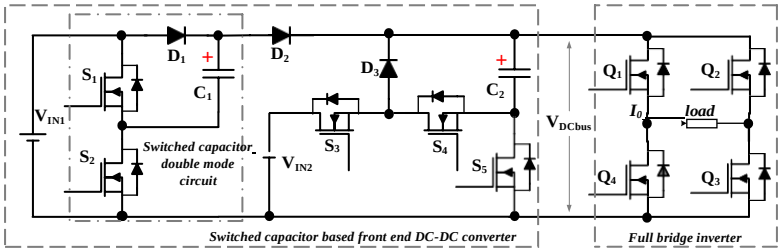
INTRODUCTION

High Frequency Alternating Current Power Distribution Systems (HFAC PDS) offer numerous benefits over conventional DC PDS. Principle advantage is that HFAC PDS omits the rectifier and a filter stage in front end, and an inverter stage in the point of load power supply [1]. The reduction in the number of power processing stages reflects as improved efficiency, fewer component count, higher reliability and lower cost. NASA, in 1980s, initiated research in HFAC PDS for their space station [2]. HFAC PDS have features that make them attractive to aerospace, telecommunication, lighting, computer power supply, micro-grids and automotive applications [1]–[8]. A HFAC PDS includes a HFAC source, a distribution track and point-of-load converters. This paper focuses on employing a switched-capacitor multilevel inverter (SCMLI) as an HFAC source. Renewable energy farms have several DC sources, usually batteries. These inverters can effectively be utilized in such renewable energy based microgrids as it employs multiple DC input sources of different magnitude. HFAC PDS employing compact transformers, smaller filters and high density power converters offer several advantages to the micro-grids user [8]. HFAC distribution enables to filter out higher order harmonics relatively easily. Major hindrance for HFAC power distribution is the higher ohmic losses due to skin and proximity effects, and magnified impedance across the transmission line. Both these factors increase with increase in length of distribution and distribution frequency.

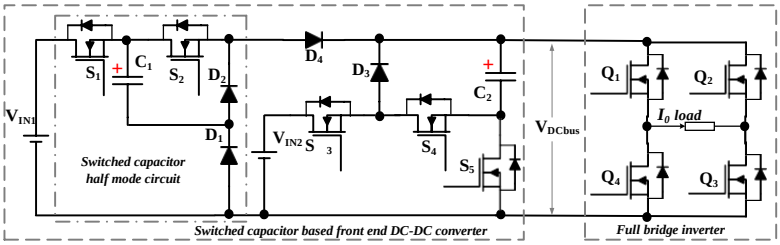
Multilevel inverters (MLI) have attained wide acceptance owing to the exciting features they offer. MLI output stair-case waveforms which greatly mitigates the harmonic content when compared to traditional square wave inverters. MLI are generally classified into diode clamped, capacitor clamped (also referred to as flying capacitor) and cascaded multilevel inverters [9], [10]. Diode clamped MLI require many addi- tional diodes as the level increases, the capacitor voltages are unbalanced and the voltage rating for the blocking diodes is high. Capacitor clamped MLI also suffer

from voltage imbalance and require several additional storage capacitors as the voltage level increases which makes it more expensive and difficult during the package process. The major drawback in cascaded MLI is the necessity for separate isolated DC sources.

There has been growing interest in Switched-Capacitor Multilevel Inverters (SCMLI) over the past few years [11]–[26]. A seven-level SCMLI using series-parallel conversion employing a single DC source with comparison of level and phase-shifted PWM is presented in [11]. A generalized single- source step-up SCMLI capable of driving inductive loads is presented in [12]. A novel SCMLI proposed in [13] also utilizes a single DC source to obtain a voltage stepup. In [14], [15], an SC doubler circuit is employed with traditional cascaded H-bridge to obtain a relatively higher voltage step count with fewer components in comparison to the traditional cascaded MLI. The partial charging of SC technique discussed in [16] is relatively complicated as it is difficult to control the



(a) Proposed topology A



(b) Proposed topology B

Fig. 1: Two basic proposed structures of SCMLI employing (a) SC voltage double mode circuit (b) SC voltage half mode circuit

charging profile of the boost SCMLI. In [17], a multi-source step-up SCMLI with reduced component count capable of driving inductive loads is presented. Similarly, in [18], multiple sources are utilized along with a single SC cell to realize a stepup SCMLI. A capacitive voltage divider technique is used to obtain a nine-level SCMLI in [19]. In [20], a novel SC cell with two capacitors in parallel with a DC source is proposed to realize a boost SCMLI capable of driving R-L loads. A hybrid nineteen-level MLI utilizing the features of both SC and flying capacitor technique is presented in [21]. In [22], the SCMLI utilizes the bipolar series-parallel or cross- switched SC technique to charge the switched-capacitors and to step-up the voltage. Asymmetric voltage sources are used to derive multilevel output voltage waveform without stepping up in [26].

SCMLI topologies in [11], [13], [19] employ a single voltage source to realize higher number of output voltage levels whereas [18], [23], [24], [26] employ multiple DC voltage sources. However, both these types operate by charging the parallel SC to input voltage and discharging it while connecting in series to the load. SCMLI are relatively more apt to high frequency output AC inverters [13] as the size of the energy storage capacitor at high frequency is small and the quality of output waveform is better with low distortion. Several switching techniques including phase shift [14], SHE [13], [24], level and phase shifted PWM [11] for SCMLI have been studied.

To realize a high frequency AC micro-grid of a few kWs, it is crucial to employ power converters with fewer components to realize a cost effective system with higher reliability. With the proliferation in renewable energy based solar and wind farms, such multi-input topologies gain tremendous potential. This would make it easier to convince the customers to partic- ipate; for example to install roof top solar panels with HFAC (or even LFAC) PV inverters. This new family of inverters naturally tend to use fewer components to realize a multilevel staircase output when compared to traditional topologies of MLI. Additionally, their operation principle charges the DC capacitor to a finite voltage each half cycle, which solves the voltage imbalance issue. However, there is a limitation on the power level these inverters

can operate at. This limitation is due to the fact that the DC capacitor employed is used to feed the load during certain intervals of operation and there is an inherent limitation to it due to the voltage ripple. Also, at higher power levels, the size of the capacitor becomes larger. Higher capacitance also leads to spiky charging currents which can impact the life of a capacitor and lead to significant EMI issues.

TOPOLOGIES FOR HFAC MICROGRIDS

Both the SCMLI topologies discussed in the following subsections are derived from [24]. The first topology (Fig.1a) increases the number of output voltage levels by employing an SC doubler circuit by cascading it with a voltage source. The second topology (Fig.1b) employing SC half circuit to increase the voltage levels. Both these basic nine-level topologies are generalized (Fig.4a and 4b).

Topology A description and operation principle

In the proposed SCMLI topology A shown in Fig. 1a, front end SC based DC-DC converter employs two input sources (V_{IN1} and V_{IN2}), five transistors (S_1, S_2, S_3, S_4 and S_5), three diodes (D_1, D_2 and D_3) and two capacitors (C_1 and C_2). DC levels obtained at the inverter DC bus include V_{IN1},

$2V_{IN1}$, V_{IN2}, $V_{IN1} + V_{IN2}$. The H-bridge inverter employing
(V_{IN1}, $2V_{IN1}$, V_{IN2}, $(V_{IN1}+V_{IN2})$) and a zero across transistors that the switches and the voltage sources employed are ideal;

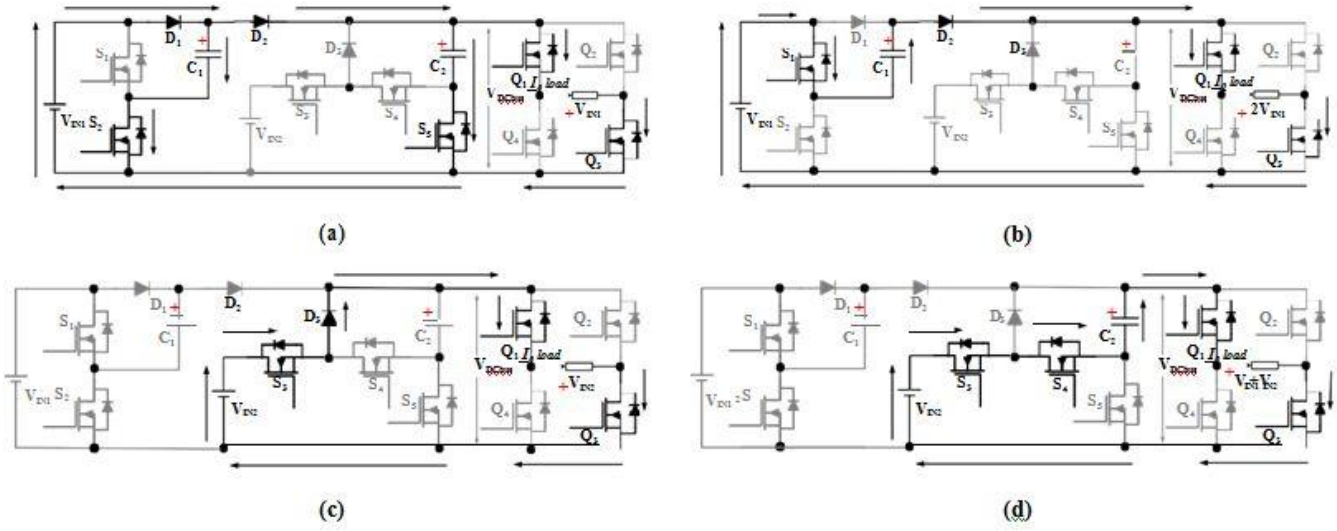


Fig. 2: Equivalent circuits of the proposed 9-level SCMLI to obtain different voltage levels (a) $V_o = V_{IN1}$ (b) $V_o = 2V_{IN1}$ (c) $V_o = V_{IN2}$ (d) $V_o = VIN\ 1 + VIN\ 2$

Capacitances (C_1 and C_2) are large enough to maintain a constant voltage and supply constant output current, and the voltage ripple across them is small enough to be neglected. Table 1 explains the switching logic of the proposed inverter. The working states are explained in the following subsections. In general, to obtain a positive voltage across the load, H- bridge transistors Q_1 and Q_3 are turned ON. Similarly, to obtain a negative voltageacross the load, transistors Q_2 and Q_4 are turned ON.

Table I: Switching logic for the proposed topology A

S_1	S_2	S_3	S_4	S_5	V*DCbus*
0	**1**	0	0	**1**	V*IN* 1
1	**0**	0	0	**0**	2V1*N* 1

0	**0**	1	0	**0**	V*IN* 2
0	**0**	1	1	**0**	V*IN* 2+V*IN* 1
0	**1**	0	0	**1**	0

Table II: Switching logic for proposed topology B

S_1	S_2	S_3	S_4	S_5	V*DCbus*
1	0	0	0	1	$0.5V_{IN1}$
1	1	0	0	0	V*IN* 1
0	0	1	0	0	V*IN* 2
0	0	1	1	0	0.5V*IN* 1+V*IN* 2
0	1	0	0	1	0

1) *Output voltage* ± V_{IN1} *state:* Capacitor C_1, is charged equal to the input voltage source V_{IN1} through D_1 by turning ON transistor S_2, while capacitor C_2 is charged to V_{IN1} by turning ON transistor S_5, through diodes D_1 and D_2. Transistors S_1, S_3, S_4 and diode D_3 remain turned OFF. The DC bus voltage at this state is equal to V_{IN1} as V_{IN2} is blocked by OFF transistor S_3. Fig. 2(a) depicts the equivalent
2) state for $V_0 = +V_{IN1}$.
3) *Output voltage* = 2 V_{IN1}
4) *state:* Transistor S_1 is turned ON, while S_2 is OFF, which connects V_{IN1} in series with capacitor C_1 (charged to V_{IN1}) and diode D_2. At this state, V_{DCbus} is equal to $2V_{IN1}$. Transistors S_3, S_4 and S_5 remain

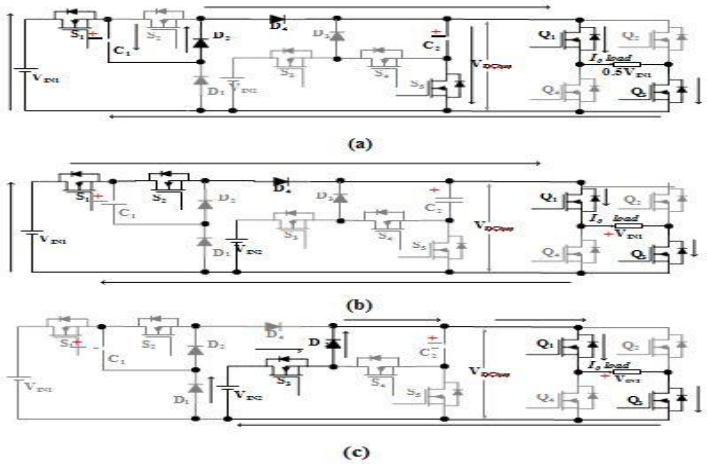


Fig. 3: Equivalent circuits of the proposed 9-level SC MLI to obtain different voltage levels (a) $V_o = 0.5V_{IN1}$ (b) $V_o = V_{IN1}$ (c) $V_o = V_{IN2}$ (d) $V_o = 0.5V_{IN1} + V_{IN2}$ (e) Zero state and balancing voltage of capacitor C_1 and C_2 and 100V (Table I). If $V_{C2} = 2V_{IN1}$, the output voltage then the output voltage steps would be 20V, 40V, 60V would have a higher step up ratio, however, the THD would be slightly poorer due to non-equal voltage steps as validated in section III of the paper.

Topology B description and operation principle

In the proposed SCMLI of Fig. 2, front end SC based DC- DC converter employs two input sources (V_{IN1} and V_{IN2}), five transistors (S_1, S_2, S_3, S_4 and S_5), four diodes (D_1, D_2, D_3 and D_4) and two capacitors (C_1 and C_2). DC levels

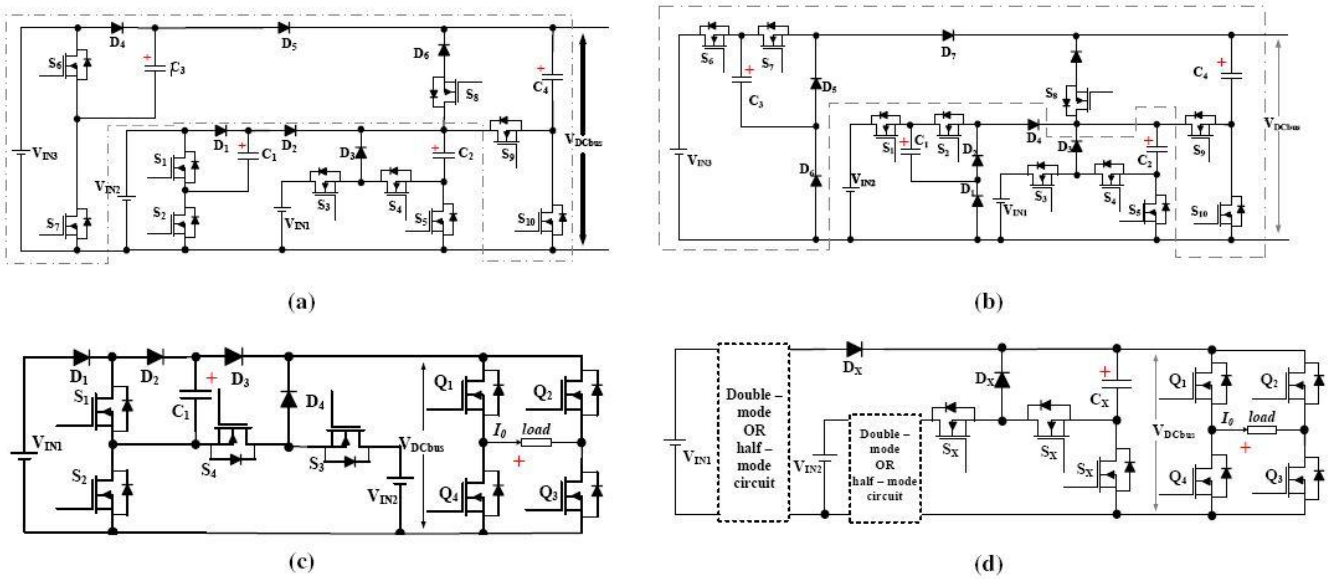


Fig. 4: (a) Generalized topology A with asymmetric sources. (b) Generalized topology B with asymmetric sources. (c) Modified topology A with fewer transistors and SCs. (d) General structure for SCMLI combining both half-mode and double mode SC converters.

Table III: Switching logic for the generalized topology for Fig. 1a

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	VDCBUS
0	0	0	0	0	0	1	0	0	1	VIN3
0	0	0	0	0	1	0	0	0	0	2VIN3
0	1	0	0	1	0	0	1	0	0	VIN2
1	0	0	0	0	0	0	1	0	0	2VIN2
0	0	1	0	0	0	0	1	0	0	VIN1
0	0	0	0	0	0	0	0	1	0	VIN3 + VIN2
0	0	1	0	0	0	0	0	1	0	VIN3 + VIN1
0	0	1	1	0	0	0	1	0	0	VIN2 + VIN1
1	0	0	0	0	0	0	0	1	0	2VIN2 + VIN3
0	0	1	1	0	0	0	0	1	0	VIN1 + VIN2 + VIN3

In the proposed topology A, shown in Fig. 1a, it can be observed that the switches S2 and S5 have identical switching logic (highlighted in Table I). Additionally, the SCs C1 and C2 are charged to the same voltage VIN1. This provides an opportunity to merge both the switches and utilize a single SC to realize a nine-level output. Fig. 4c presents a modified topology eliminating one transistor (S5) and an SC from the original topology A without sacrificing the number of output voltage levels. This innovation results in the cutting down the cost and the size of the inverter.

Fig.4d depicts a generic way of increasing the number of output voltage levels by inserting an SC double-mode or a half-mode circuit. Any one of the SC circuit can be cascaded to either of voltage sources to realize higher output voltage levels.

D. Comparisons with other proposed topologies

For the topology in Fig. 4a, the number of output levels are increased by inserting SC doubler circuitry to additional volt-

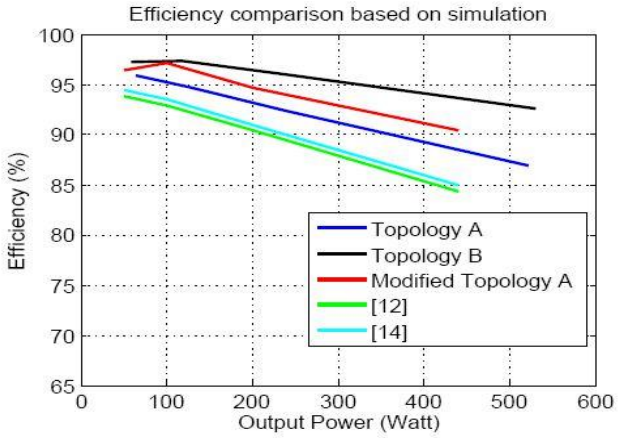


Fig. 5: Efficiency comparison of different topologies using simulation

age sources whereas for topology in Fig. 4d, SC half circuitry is employed. Employing an SC doubler circuit increases the step-up capability of the SCMLI enabling relatively higher voltage operations thereby utilizing all the advantages of a lower current system. However, it also relatively increases the voltage stress of the H-bridge. Fig.4c shows an innovative way

TABLE IV: Switching logic for the generalized topology for Fig. 1b

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_{DCBUS}
0	0	0	0	0	1	1	0	0	0	V_{IN3}
0	0	0	0	0	1	0	0	0	1	$0.5\ V_{IN3}$
1	1	0	0	1	0	0	1	0	0	V_{IN2}
1	0	0	0	0	0	0	1	0	0	$0.5\ V_{IN2}$
0	0	1	0	0	0	0	1	0	0	V_{IN1}
1	0	0	0	0	0	0	0	1	0	$0.5\ (V_{IN3}+ V_{IN2})$
1	1	0	0	0	0	0	0	1	0	$0.5\ V_{IN3} + V_{IN2}$
0	0	1	1	0	0	0	1	0	0	$V_{IN1} + 0.5\ V_{IN2}$
1	0	0	0	0	0	0	0	1	0	$V_{IN1} + 0.5\ V_{IN3}$
0	0	1	1	0	0	0	0	1	0	$V_{IN1} + 0.5\ V_{IN2} + 0.5\ V_{IN3}$

to reduce the active switches and SC count in the proposed inverter based on SC doubler (Fig.1a). In Table V, several proposed SCMLI structures are compared with respect to the number of active switches (nT) and diodes(nD) used, number of output levels (nl) generated and the number of voltage sources (i) by choosing the number of switched-capacitors employed (n) as the reference. It is seen that the proposed SCMLI offers a good trade-off between the number of components employed to the output levels generated. In Table VI, multi-input SCMLI topologies with symmetric output voltage levels are compared using costfunction (CF), similar to the cost function analysis proposed in [17], [20]. The cost function in the above equation takes into account the number of transistors and drivers, diodes, DC sources and SCs. For simplicity, the number of drivers is assumed to be equal to the number of transistors and written as 2nT . From Table VI, it can be seen that proposed family of SCMLI havea CF in the similar range with the Modified Topology A having the least CF. The topology from [20] and the Modified Topology A offer the least CF which means that they produce higher number of symmetric output voltage levels with fewer components. Most SCMLI topologies in the literature, including the proposed family, employ fewer semiconductor switches and capacitors when compared to traditional MLI. The novel Fibonacci inverter proposed in Fig.2 of [25] uses fewer components than the conventional inverter. However, the proposed SCMLI employs relatively fewer components even when compared to the novel Fibonacci inverter. For example, to realize a 15-level inverter (7 x step up) the novel Fibonacci inverter employs eight SCs, twenty four transistors and six diodes with a single voltage source. In comparison, the proposed inverter can obtain twenty-one levels with only four SCs, fourteen transistors, six diodes and three asymmetric voltage sources.

The ability of the proposed family of inverters to drive large inductive loads is restricted. This limitation can be observed from the topology. This is because there is no path for the inductor current to flow to the ground during certain intervals. The maximum angle between the voltage and current can only be _1 (Refer Fig.6), similar to the topologies in [13], [24]. However, topologies proposed in [12], [17], [20] can drive large inductive loads. This is one shortcoming of

the proposed family of SCMLI. The efficiency comparison is carried out in Fig.5 for different nine level inverters under pure resistive loading. To obtain a fair comparison, the following parameters and non-idealities were chosen. RdsON = 0:09, Rin = 0:1, ESR = 0:05, Rd = 0:05, VF = 0:42V , C = 1000_F and fS = 400Hz. The peak voltage for all topologies was adjusted to _80 V with steps of _ 20 V. All the topologies were switched using staircase modulation. The common trend is that the efficiency drops as the power increases. Another observation is that with increase in the number of switches, and especially SCs, the fall in efficiency is higher. The proposed family of SCMLI utilizes the SC voltage only to obtain very few output voltage levels when compared to single source SCMLI proposed in [12], [13], [15], [17]–[19]. For example, topology A and B utilizes the SC voltage directly in four out of nine output voltage levels. The remainder levels are directly supported by the voltage source. In comparison, the topology proposed in [12], having the least efficiency among the compared ones, utilizes the SC voltage in five out of seven voltage levels. This allows the proposed family of SCMLI to operate at a comparatively higher efficiency as the loss effect from SC ripple voltage is mitigated.

MODULATION STRATEGIES FOR THE PROPOSED SCMLI

Pulse width modulation (PWM) techniques for inverters can be broadly categorized into carrier based high frequency switching PWM and fundamental switching frequency based PWM. In high frequency switching PWM, the switching losses are severe as the transistors and diodes are commutated several times per switching cycle. In the case of fundamental switching frequency based PWM, the transistors are commutated just once or twice per switching cycle. This reduces switching loss considerably.

RESULTS

The parameters are listed in Table IX. Simulation results, for the proposed topology A, depicting the output voltage and current waveforms and SC voltage and current waveforms are shown in Fig. 11. The simulation is carried out at MI = 0.8 for both SHE and minimum THD with equal steps. The FFT waveforms for SHE and minimum THD with equal steps are depicted in Fig. 11c and Fig. 11d respectively. Under SHE, the 5th and 7th harmonic are minimized to 0.5 V and 0.4 V respectively. The harmonics are not equal to zero since non-ideal components are employed during simulations. Additionally, the switching angles have decimal points and are difficult to emulate during simulations. For minimum THD with equal steps the THD is relatively lower than that under SHE. This confirms the theoretical evaluation and plots in and Fig. 7c and Fig. 8c. Experiment verification for topology A is carried out with the same parameters. The voltage and current waveforms of the output and the SC operating at 400 Hz are shown in Fig. 12. Fig. 13 show the waveforms at different output power frequency and power levels. At higher power levels, the voltage droop in the output waveform is higher due to higher voltage ripple (plotted in Fig. 17b). However, the ripple proportionately reduces with increase in the output frequency for a given value of capacitance as explained in (17). FFT of the output voltage for SHE modulation is shown in Fig. 14a. The digital oscilloscope displays the RMS value of the amplitude of different frequency components. The 5th, 7th and 11th harmonic are minimized (around 1 V) similar to the simulation results. FFT results for minimum THD modulation is shown in Fig. 14b. The 3rd, 5th and 7^{th} harmonics are comparatively larger when compared to the SHE modulation scheme, similar to theoretical and simulation observations. FFT results under minimum THD scheme with unequal voltage steps (Fig. 14c) show higher value of lower order harmonics in comparison. The proposed SCMLI topology A is tested with different RL loads and the waveforms are shown in Fig. 15. Fig.15a and 15b depict 400 Hz waveforms of output voltage and current

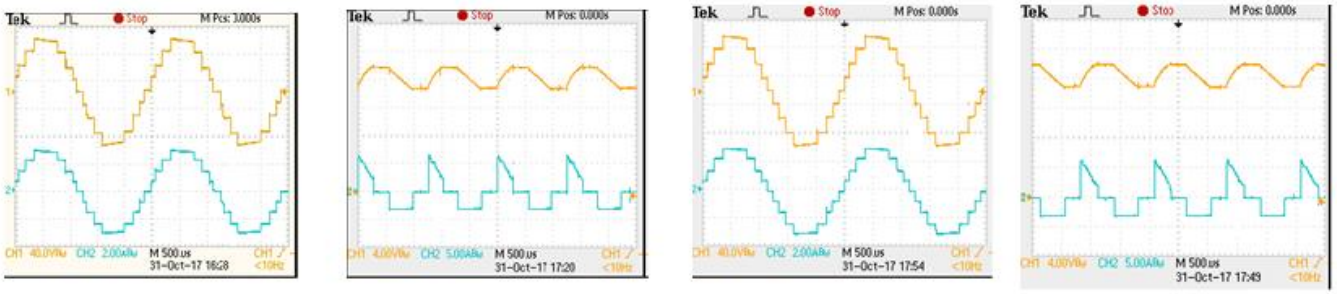


Fig. 12: Experimental results operating at fS = 400 Hz. (Ch.1 - Voltage, Ch.2 - Current) (a) Output voltage and current under SHE (MI = 0.8) (b) switched capacitor voltage and current under SHE (d) Output voltage and current under Min. THD technique operating with equal voltage steps (MI = 0.82) (e) switched capacitor voltage and current under Min. THD technique operating with equal voltage steps

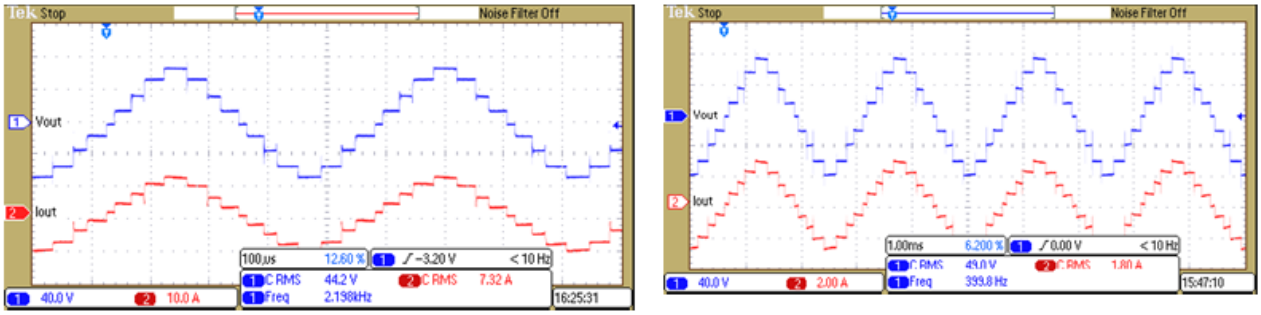


Fig. 13: Experimental results (a) Output voltage and current at 400 Hz with output power of 88 W (b) Output voltage and current at 2200 Hz with output power of 320 W [23]

driving a 25 -220 _H and 16.7 -220 _H load respectively. Fig.15c and 15d depict 400 Hz waveforms of output voltage and current driving a 25 -440 _H and 16.7 -440 _H load respectively. It can be observed that the current waveforms driving the 440 _H load is more sinusoidal. The ability of the proposed SCMLI to drive loads with larger inductance value is limited as discussed in section II D. The dynamic loading experiment is performed on topology A and the results are shown in Fig.16. In Fig.16a and 16b, initially the SCMLI is driving a pure 25 load. Another pure 50 is added in parallel using a switch to increase the load current by approximately 50%. Similarly, in Fig.16c and 16d, initially the SCMLI is driving a pure 16.7 (25 in parallel with 50) load. The 50 is removed from the current path by opening the switch to lower the load current by 33%. It is seen that under both scenarios the SCMLI responds well. Fig. 17a shows the measured plot of efficiency versus output power at different output frequencies. Fig. 17b shows the measured plot of capacitor (C2) peak to peak ripple versus output power at different frequencies. With increase in frequency, the peak to peak capacitor voltage reduces. This in turn reduces the conduction loss in the capacitor and contributes to higher efficiency. The efficiency drops with increase in output power. This can be mitigated by employing larger switched capacitors, designing zero voltage switching or zero current switching front end converters and by choosing transistors with low Rds ON, diodes with low Vf .

CONCLUSIONS

This article For high frequency AC applications, a family of SCMLI topologies are suggested in this article. The used asymmetric sources share a common ground, allowing for a more straightforward design. The inherent capacitor voltage imbalance issue that plagues conventional MLI is resolved by the capacitors being charged every half-cycle. The two proposed topologies' operating principles are thoroughly explored, along with recommendations for enhancements. A generalised topological structure is created, and it is contrasted with a number of current topologies. Table V demonstrates that, in terms of the amount of components required to produce a given number of voltage levels, the proposed SCMLI offers a good trade-off. Such inverters are quite helpful in circumstances where there are many DC sources available, such as in the case of farms that produce renewable energy. Instead of connecting several DC source fed inverters in parallel, it is preferable to use numerous DC sources as input to a single inverter in order to generate higher power. We looked at two alternative staircase modulation techniques: time-domain minimum THD schemes and frequency domain selective harmonic removal. Even when the output voltage waveform steps are not equal, the minimum THD approach can be applied. Three versions of the aforementioned staircase modulation techniques are shown in a number of switching angle versus modulation indices charts. The reader may see from these charts how switching angles normally change with modulation index. To further understand how THD varies with modulation index, THD values for the relevant switching angles are calculated and shown against those indices then plotted against modulation indices to better comprehend the relationship between THD variation and modulation indices, as well as the area of the plot where the THD is lowest. Under both modulation strategies, the suggested topology A is put to the test. The experimental findings support the conclusions of the simulation and theory.

REFERENCES

[1]. Jain, P., Pahlevaninezhad, M., Pan, S., and Drobnik, J.. “A Review of High Frequency Power Distribution Systems: for Space, Telecommunication, and Computer Applications”,IEEE Transactions on Power Electronics, pp. 3852 - 3863, Vol. 29, Issue 8, 2014.
[2]. ”Status of 20 kHz Space Station Power Distribution Technology”, NASA Publication, TM 100781.
[3]. S. R. Raman and K. W. E. Cheng, ”Ideas for future electric aircraft system,” 2015 6th International Conference on Power Electronics Systems and Applications (PESA), Hong Kong, 2015.

[4]. J. Drobnik, "High frequency alternating power distribution for telecommunication systems", in Proc. IEEE INTELEC94, 1994, pp. 174182.
[5]. Raghu, Raman S., Junfeng Liu, X. D. Xue, and KW Eric Cheng, "High frequency AC auxiliary power source for future vehicles" 2015 6th International Conference on Power Electronics Systems and Applications (PESA), Hong Kong, 2015.
[6]. Seng-Yim Ng; Luk, P.C.; Jinupun, K., "High frequency AC distributed power system for fluorescent lighting" Power Electronics and Applications(EPE 2011), Proceedings of the 2011-14th European Conference on, Aug. 30 2011-Sept. 1 2011.
[7]. Wennan Guo; Jain, P.K., "A power-factor-corrected AC-AC inverter topology using a unified controller for high-frequency power distribution architecture", IEEE Transactions on Industrial Electronics, vol.51, no.4, pp. 874-883, Aug. 2004.
[8]. S. Chakraborty, M. D. Weiss and M. G. Simoes, "Distributed Intelligent Energy Management System for a Single-Phase High-Frequency AC Microgrid," in IEEE Transactions on Industrial Electronics, vol. 54, no. 1, pp. 97-109, Feb. 2007.
[9]. J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications", in IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, Aug 2002.
[10]. Kouro, Samir, Mariusz Malinowski, K. Gopakumar, Josep Pou, Leopoldo G. Franquelo, Bin Wu, Jose Rodriguez, Marcelo A. Perez, and Jose I. Leon., "Recent Advances and Industrial Applications of Multilevel Converters" in IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.
[11]. A. Tsunoda, Y. Hinago and H. Koizumi, "Level- and Phase-Shifted PWM for Seven-Level Switched-Capacitor Inverter Using Series/Parallel Conversion," in IEEE Transactions on Industrial Electronics, vol. 61, no. 8, pp. 4011-4021, Aug. 2014.
[12]. Y. Hinago and H. Koizumi,"A Switched-Capacitor Inverter Using Series/ Parallel Conversion With Inductive Load," in IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 878-887, Feb. 2012.
[13]. Y. Ye, et. al., "A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing," in IEEE Transactions on Industrial Electronics,vol. 61, no. 12, pp. 6672-6680, Dec. 2014.
[14]. J. Liu, K. W. E. Cheng and Y. Ye, "A Cascaded Multilevel Inverter, Based on Switched-Capacitor for High-Frequency AC Power Distribution System," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4219-4230, Aug. 2014.
[15]. E. Babaei and S. S. Gowgani, "Hybrid Multilevel Inverter Using Switched Capacitor Units," in IEEE Transactions on Industrial Electronics, vol. 61, no. 9, pp. 4614-4621, Sept. 2014.
[16]. M. S. W. Chan and K. T. Chau,"A New Switched-Capacitor Boost- Multilevel Inverter Using Partial Charging," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 12, pp. 1145-1149, Dec. 2007.
[17]. Barzegarkhoo, Reza, Hossein Madadi Kojabadi, Elyas Zamiry, Naser Vosoughi, and Liuchen Chang, "Generalized Structure for a Single Phase Switched-Capacitor Multilevel Inverter Using a New Multiple DC Link Producer With Reduced Number of Switches" in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5604-5617, Aug. 2016.
[18]. Fong, Y. C., Yuanmao Ye, S. Raghu Raman, and K. W. E. Cheng, "A Hybrid Multilevel Inverter Employing Series-parallel Switched-capacitor ric hybridised design for a novel step-up 19-level inverter," in IET Power Electronics, vol. 10, no. 11, pp. 1377-1391, 2017. Unit," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017.
[19]. J. Liu, J. Wu, J. Zeng and H. Guo, "A Novel Nine-Level Inverter Employing One Voltage Source and Reduced Components as High- Frequency AC Power Source," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2939-2947, April 2017.
[20]. R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, H. Madadi Kojabadi and F. Blaabjerg, "A New Boost Switched-Capacitor Multilevel Converter With Reduced Circuit Devices," in IEEE Transactions on Power Electronics, vol. 33, no. 8, pp. 6738-6754, Aug. 2018.